A TECHNIQUE FOR SHIPBOARD SONAR ECHO SIMULATION FOR TRAINING

NAVAL TRAINING EQUIPMENT CENTER

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Naval Training Equipment Center
Orlando, Florida 32813

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June 1976

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20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

A means for synthesizing echoes using a combination of analog and digital techniques for target classification training of shipboard ASW men was needed.

A study indicated that the echoes could be generated by using the latest state-of-the-art methods and components.

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A system incorporating solid state components was designed and implemented to produce a synthetic sonar echo. The finalized research tool was then evaluated at the Key West Fleet Sonar Training School and at the Naval Training Equipment Center, Orlando. Installation of a prototype trainer in a Navy Sonar Training School is recommended. Training effectiveness studies should be conducted in order to determine the full extent of training transfer from the simulator to the real world situation. It is further recommended that this study be continued to include the effects on the echo signal due to multipath propagation and reverberation. Methods should be investigated to feed the echo signal to the sonar set receiver processor input on a non-programmed basis. This would include additional electronics or a mini-computer to solve target motion and position relative to own ship.

PREFACE

Existing shipboard echo generators are not suitable for classification training. A need has existed for means whereby shipboard operator training in active sonar target detection and classification could be accomplished. Such echo simulators are desirable for use in place of mobile targets or submarines to track in training exercises, in decoy devices for misleading enemy antisubmarine measures, and in shorebased sonar training devices. With this in mind, it was a principal object of this task to provide a simulator utilizing a novel combination of digital and analog techniques to generate a simulated echo. This simulated echo is a function of target characteristics, i.e., length, aspect angle, doppler frequency.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

SECTION I

INTRODUCTION

This report documents results of a study to determine the effectiveness of a shipboard target classification trainer, efforts included:

a. Analyzing immediate sonar training problems

b. Study of present target generation techniques

c. Investigated work being done by other facilities in government, universities, and industries.

d. Generation of preliminary system design.

e. Investigation of latest state-of-the-art design techniques for analog, digital, and memory systems.

f. Finalized design, construction, and testing of research tool.

SECTION II

STATEMENT OF THE PROBLEM

A need exists for a means whereby shipboard operator training in active sonar target detection and classification could be accomplished. Such echo simulators are desirable for use in mobile targets for submarines to track in training exercises, in decoy devices for misleading enemy antisubmarine measures, and in stationary type sonar training devices. With this in mind, a sonar echo simulator was designed for the purpose of synthesizing echoes by utilizing a novel combination of analog and digital techniques to generate the simulated echo.

SECTION III

PROCEDURE

The concept of generating a simulated sonar echo is as follows: The simulator must contain a computer that solves for: Echo length and amplitude versus-

a. Target length

b. Angle of target relative to oncoming signal, i.e., aspect angle.

c. Frequency of echo versus velocity of target relative to ship i.e., Doppler.

The solution is dependent upon some initial normalized source level, transmitted pulse length, the appropriate parameters of sonar transmission and target reflection. Answers to the following questions must be provided before simulation can be accomplished:

a. What are the parameters that must be simulated in the target echo return?

b. What are the electronic techniques that may enable the implementing of these techniques?

This report covers the answers to the above questions, and extensive investigations have been performed on the transmissions of sound in the ocean and on target echo returns.

From footnote 1, data was given that showed the effect of target echoes relative to:

a. Highlight strength as a function of aspect angle.

b. Target strength as a function of aspect angle.

c. Echo length as a function of aspect angle

From footnote 2, information was obtained that showed the effects of echo return relative to:

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1 R. Rubega, Description of Target Strength Parameters Important to Echo Simulation (New York: Marine Resources, Inc. Oct 1968) Document #858/69/1

2 R. J. Urick, Principles of Underwater Sound for Engineers

a. Target length

b. Aspect length

c. Relative velocity for Doppler shift

The two references set the parameters for the target echo. Now what was needed was a method of implementing them electronically.

Two electronic methods were to be tried to simulate the target echo. (Refer to footnote 3).

a. An electronically variable, tapped delay line.

b. Storage of the sonar pulse in a memory, and reading the signal out at some delayed time to simulate target range.

The two methods were partially combined into one approach for budgeting purposes.

The electrical sonar signal is first digitized and then stored in a memory. When the target return is due, the memory is read out and fed into the electronically variable delay line. This line consists of many series shift registers (SR) having multiple taps.

These taps represent the highlights of the echo signal, and also give the necessary controlling of the echo length. The gain of the total summed signal is digitally controlled as a function of aspect angle to give the correct relative amplitude return. The frequency of the echo signal varies as a function of relative velocity by controlling a beat-frequency mixing circuit. A detailed description of the system follows with schematics of each phase shown as figures 1 to 21.

3 Murphree, Francis, Sonar Echo Simulator, U. S. Patent #3,610,798, October 1971

SECTION IV

SONAR ECHO SIMULATION SYSTEM

EXTERNAL INPUTS

a. Keying Gate of transmissions output signal

b. Trigger pulse to simulate target distance

c. Transmission output signal (low level)

PANEL CONTROL

a. Aspect Angle

b. Target Length

c. Target Velocity

SECTION V

SYSTEM ANALYSIS

SIGNAL FLOW

A low-level sample of the transmission output signal feeds into operational amplifier (op amp) follower with an input impedance of 100K onms (figure 4).

The amplifier output is fed into a mixer and voltage-controlled oscillator (VCO) that beats the input signal with the frequency of the oscillator. The resultant mixed frequencies are fed into a low pass filter of 40 db/octave (figure 5).

The low frequency signal is digitized at a 7500Hz rate, inverted, then fed as a 6 bit-word, having a resolution of 150 mv, to either a solid state memory, or directly to shift registers (figure 6).

The shift registers (S/R) consist of thirty 32 x 6 bit chips that control the length of the echo signal. Each S/R chip represents 10 feet of target length. A target of 10-300 feet can be simulated (figure 6).

The output of each 6-bit S/R is fed into a digital to analog (D/A) device to change the signal back into the analog form. Each D/A can be sequentially turned on or off to shorten the simulated echo.

All outputs are then fed into summing op amps having a gain that is a function of aspect angle (figure 13).

This signal is then fed into a mixer and VCO. The oscillator frequency is a function of velocity and simulates doppler effects.[2]

$$\Delta f = 2 \frac{v}{c} f$$

where: v is the relative velocity

f is the transmitted frequency

c is the velocity of sound in water

Δf is the change in frequency

In practical terms, and for a sound velocity of 4900 ft/sec.

$\Delta f \approx \pm 0.7$ Hz/Knot KHz

The mixed signal is fed into a bandpass filter with a roll-off of 40 db/octave and resulting signal fed to an output op amp. The output of this amplifier is the simulated sonar echo and is a function of target length doppler, and aspect angle, [1]

$$\text{Echo Length} = \tau + \frac{2L}{C} \cos \theta$$

where: τ is the length of the transmitted signal

L is the target length

θ is the aspect angle

The input resistance to the op amp is a function of target distance and varies the echo signal amplitude.

SECTION VI

PANEL CONTROLS

ASPECT ANGLE

This is a setting of a potentiometer, or may be a computer-controlled voltage that is fed through a buffer op amp to a 5 bit output Analog to Digital (A/D converter.

The output of the A/D is then fed to read-only memories (ROMs) Nos. 1, 2, and 4; each ROM having a 32 x 8 bit word (figure 7)

ROM No. 1 has 3 bits going to a UNIT readout (r/o lamp, 4 bits to a TENS r/o lamp and 1 bit to a HUNDREDS r/o lamp. These readouts visually indicate aspect angle.

ROM No. 2 has 1 bit going to the HUNDREDS r/o, 2 bits to analog switches that control aspect angle gain, and 5 bits to a D/A that feeds one input of the length control multiplier.

ROM No. 4 has its full 8 bits feeding a D/A that has a 4 millivolt resolution.

The output of the D/A feeds an op amp follower and then to one input of the velocity control multiplier.

VELOCITY CONTROL

This is a setting of a potentiometer, or may be computer-controlled voltage that is fed to one input of the velocity multiplier.

The output of the multiplier feeds a summing op amp. One input is set for the center frequency voltage when the velocity input is zero.

The output of the op amp is the dc voltage for controlling the VCO that simulates doppler.

LENGTH CONTROL

This is a setting of a potentiometer or may be a computer-controlled voltage that feeds a dc voltage to a buffer op amp follower.

The output of the op amp goes to one input of the length multiplier and the multiplier output goes to another op amp follower (figure 12)

The output of the follower goes to a 5-bit D/A with a resolution of 33 mV, and the output of the D/A goes to ROM No. 3 (figure 9).

SECTION VII

RANDOM ACCESS SOLID STATE MEMORY

The Random Access Solid State Memory (RAM) consists of forty-eight 1024 x 1 bit chips that are wired to perform as an 8192 x 6-bit word memory device (figure 18)

The timing and controls for the RAM are an important part of this design and an explanation follows (figure 17)

At the time of the sonar transmission, a gate is monitored from the electronics of the sonar. This gate is fed to an op amp having an input impedance greater than 10 meg-ohms. The output of the op amp feeds the transmission gate to the UP/DOWN input at a counter, an OR gate, two one-shot chips, and an inverter state.

At the start of transmission, a one-shot resets the 4 state counter before counting begins. The one-shot has a complimentary output that goes to a NOR gate that resets the 10-bit address counter and the 3 bit counter through an OR-Gate circuit. The 4 state counter starts counting a 7500 Hz clock at the start of transmission, and stops the count at the end of transmission. This final count determines the length of the transmitter sonar signal. At the same time the 10-bit counter addresses the memory, in a "write" mode, and stores the digitized sonar signal. At every count of 1024, this counter feeds a signal into a one-shot that resets the counter and steps the 3-bit counter. The 3-bit counter supplies the logic to an 8 pole analog switch that passes a chip-select signal through driver gates. This determines the portion of the memory to be selected. The counter is reset through a one-shot and the OR-gate.

When a target is presented as an input and the transmission gate is off, a flip flop is activated that causes the 4-state counter to count-down from its present number. When the counter reaches zero, a decoder triggers a one-shot that then resets the flip-flop, gating the counter off. When the count-down begins, the 10-bit address counter and the 3-bit counter activates the memory, which has now switched to a READ mode. READ is stopped upon resetting the flip-flop. The final output signal is a function of:

1. Target Length, L
2. Doppler Frequency, Δf
3. Aspect Angle, θ

SECTION VIII

RESULTS AND RECOMMENDATIONS

The finalized research tool was evaluated at the Key West Sonar Training School, and at the Naval Training Equipment Center, Orlando. The sonar visual display was observed by several experienced sonarmen (operators/instructors) and subjectively judged to be of a realistic quality echo. Tests were performed varying the width of the sonar output signal and observing the echo displays.

Installation of a prototype trainer in a Navy sonar training school is recommended. Training effectiveness studies should be conducted in order to determine the full extent of training transfer from the simulator to the real world simulation. It is further recommended that this study be continued to include the effects on the echo signal due to multipath propagation and reverberation. Methods should be investigated to feed the echo signal to the sonar set receiver processor input on a nonprogrammed basis. This would include additional electronics or a mini-computer to solve target motion and position relative to own ship.

To summarize, this task has shown that there is a need for a shipboard echo sonar simulator. Using the newest electronic solid state technologies, the problems of shipboard space and costs can be kept down to a minimal figure which would allow sonar training at sea for all ships carrying operational sonars.

NAVTRAEQUIPCEN IH-231
APPENDIX A
PARTS LIST OF MAJOR COMPONENTS

ITEM	MANUFACTURER	PART NO.
Operational Amplifier	Fairchild	U5B741
Waveform Generator	Exar	XR-205
Filter	Kinetics	FS-61
A/D Converter	Datel	ADC-EH
A/D Converter	Datel	ECONOVERTER
D/A Converter	Datel	DAC-298
D/A Converter	Motorola	MC 1406L
Hex Inverter	Fairchild	9016
One-Shot	Fairchild	9602
Nand-Gate	Fairchild	9002
1X16 Decoder	Fairchild	93L11
Binary Counter	Fairchild	9316
Quad 2-Input AND	Fairchild	9N08
And/Or	Fairchild	9H52
Quad-Or	Fairchild	9014
Dual Flip-Flop	Fairchild	9024
UP/DOWN Decade Counter	Signetics	8285A
Shift Register, Hex 32-Bit	Signetics	2518
Read Only Memory, 32X8-Bit	Signetics	8223
Random Access Memory, 1024X1-Bit	Intel	2102
Power Supply $\pm$ 15 Volts	Acopian	TD15-250
Power Supply + 5	Acopian	B5GT500

SIGNETICS 8223, 82S23, 82S123 FIELD-PROGRAMMABLE 256-BIT (32X8) READ-ONLY MEMORIES

Read-Only Memory No. 1

PR-369 TRUTH TABLE (32 x 8)

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	OCTAL ADDR.	DEC. ADDR.
0	0	0	0	0	0	0	0	0 0 0	0
0	0	0	0	1	0	0	1	0 0 1	1
0	0	0	1	0	0	1	0	0 0 2	2
0	0	0	1	1	0	1	1	0 0 3	3
0	0	1	0	0	1	0	0	0 0 4	4
0	0	1	1	0	0	0	0	0 0 5	5
0	0	1	1	1	0	0	1	0 0 6	6
0	1	0	0	0	0	1	0	0 0 7	7
0	1	0	0	1	0	1	1	0 1 0	8
1	0	0	0	0	1	0	0	0 1 1	9
1	0	0	1	0	0	0	0	0 1 2	10
1	0	0	1	1	0	0	1	0 1 3	11
1	0	1	0	0	0	1	0	0 1 4	12
1	0	1	0	1	0	1	1	0 1 5	13
1	0	1	1	0	1	0	0	0 1 6	14
1	1	0	0	0	0	0	0	0 1 7	15
1	1	0	0	1	0	0	1	0 2 0	16
0	0	0	0	0	0	1	0	0 2 1	17
0	0	0	0	1	0	1	1	0 2 2	18
0	0	0	1	0	1	0	0	0 2 3	19
0	0	1	0	0	0	0	0	0 2 4	20
0	0	1	0	1	0	0	1	0 2 5	21
0	0	1	1	0	0	1	0	0 2 6	22
0	0	1	1	1	0	1	1	0 2 7	23
0	1	0	0	0	1	0	0	0 3 0	24
1	0	0	0	0	0	0	0	0 3 1	25
1	0	0	0	1	0	0	1	0 3 2	26
1	0	0	1	0	0	1	0	0 3 3	27
1	0	0	1	1	0	1	1	0 3 4	28
1	0	1	0	0	1	0	0	0 3 5	29
1	0	1	1	0	0	0	0	0 3 6	30
0	0	0	0	0	0	0	0	0 3 7	31

SIGNETICS 8223, 82S23, 82S123 FIELD-PROGRAMMABLE
256-BIT (32X8) READ-ONLY MEMORIES

Read-Only Memory No. 2

PR-369 TRUTH TABLE (32 x 8)

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	OCTAL ADDR.	DEC. ADDR.
0	0	1	1	1	1	1	0	0 0 0	0
0	0	1	1	1	1	0	0	0 0 1	1
0	1	1	1	1	0	0	0	0 0 2	2
0	1	1	1	0	0	1	0	0 0 3	3
1	0	1	0	1	0	1	0	0 0 4	4
1	0	1	0	0	0	0	0	0 0 5	5
1	0	0	1	0	1	0	0	0 0 6	6
1	1	0	0	0	0	0	0	0 0 7	7
1	1	0	0	0	0	0	0	0 1 0	8
1	1	0	1	0	1	0	0	0 1 1	9
1	0	1	0	0	0	0	0	0 1 2	10
1	0	1	0	1	0	1	0	0 1 3	11
1	0	1	1	0	0	1	0	0 1 4	12
0	1	1	1	1	0	0	0	0 1 5	13
0	1	1	1	1	1	0	0	0 1 6	14
0	0	1	1	1	1	1	0	0 1 7	15
0	0	1	1	1	1	0	0	0 2 0	16
0	1	1	1	1	0	0	1	0 2 1	17
0	1	1	1	0	0	1	1	0 2 2	18
1	0	1	0	1	0	1	1	0 2 3	19
1	0	1	0	0	0	0	1	0 2 4	20
1	0	0	1	0	1	0	1	0 2 5	21
1	1	0	0	0	0	0	1	0 2 6	22
1	1	0	0	0	0	0	1	0 2 7	23
1	0	0	1	0	1	0	1	0 3 0	24
1	0	1	0	0	0	0	1	0 3 1	25
1	0	1	0	1	0	1	1	0 3 2	26
0	1	1	1	0	0	1	1	0 3 3	27
0	1	1	1	1	0	0	1	0 3 4	28
0	1	1	1	1	1	0	1	0 3 5	29
0	0	1	1	1	1	1	1	0 3 6	30
0	0	1	1	1	1	1	0	0 3 7	31

SIGNETICS 8223, 82S23, 82S123 FIELD-PROGRAMMABLE
256-BIT (32X8) READ-ONLY MEMORIES

Read-Only Memory No. 3

R-369 TRUTH TABLE (32 x 8)

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	OCTAL ADDR.	DEC. ADDR.
1	1	1	1	0	0	0	0	0 0 0	0
1	1	1	1	0	0	0	1	0 0 1	1
1	1	1	1	0	0	1	0	0 0 2	2
1	1	1	1	0	0	1	1	0 0 3	3
1	1	1	1	0	1	0	0	0 0 4	4
1	1	1	1	0	1	0	1	0 0 5	5
1	1	1	1	0	1	1	0	0 0 6	6
1	1	1	1	0	1	1	1	0 0 7	7
1	1	1	1	1	0	0	0	0 1 0	8
1	1	1	1	1	0	0	1	0 1 1	9
1	1	1	1	1	0	1	0	0 1 2	10
1	1	1	1	1	0	1	1	0 1 3	11
1	1	1	1	1	1	0	0	0 1 4	12
1	1	1	1	1	1	0	1	0 1 5	13
1	1	1	1	1	1	1	0	0 1 6	14
0	0	0	0	1	1	1	1	0 1 7	15
0	0	0	1	1	1	1	1	0 2 0	16
0	0	1	0	1	1	1	1	0 2 1	17
0	0	1	1	1	1	1	1	0 2 2	18
0	1	0	0	1	1	1	1	0 2 3	19
0	1	0	1	1	1	1	1	0 2 4	20
0	1	1	0	1	1	1	1	0 2 5	21
0	1	1	1	1	1	1	1	0 2 6	22
1	0	0	0	1	1	1	1	0 2 7	23
1	0	0	1	1	1	1	1	0 3 0	24
1	0	1	0	1	1	1	1	0 3 1	25
1	0	1	1	1	1	1	1	0 3 2	26
1	1	0	0	1	1	1	1	0 3 3	27
1	1	0	1	1	1	1	1	0 3 4	28
1	1	1	0	1	1	1	1	0 3 5	29
1	1	1	1	1	1	1	1	0 3 6	30
1	1	1	1	1	1	1	1	0 3 7	31

SIGNETICS 8223, 82S23, 82S123 FIELD-PROGRAMMABLE
256-BIT (32X8) READ-ONLY MEMORIES

Read-Only Memory No. 4

PR-369 TRUTH TABLE (32 x 8)

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	OCTAL ADDR.	DEC. ADDR.
0	1	1	1	1	1	1	1	0 0 0	0
0	1	1	1	1	0	1	0	0 0 1	1
0	1	1	1	0	1	0	0	0 0 2	2
0	1	1	0	0	1	0	0	0 0 3	3
0	1	0	1	0	0	1	0	0 0 4	4
0	1	0	0	0	0	0	0	0 0 5	5
0	0	1	0	0	1	1	0	0 0 6	6
0	0	0	0	0	0	0	0	0 0 7	7
0	0	0	0	0	0	0	0	0 1 0	8
1	1	0	1	1	0	0	0	0 1 1	9
1	1	0	0	0	0	0	0	0 1 2	10
1	0	1	0	1	0	1	0	0 1 3	11
1	0	0	1	1	0	0	1	0 1 4	12
1	0	0	0	1	0	1	0	0 1 5	13
1	0	0	0	0	1	0	1	0 1 6	14
1	0	0	0	0	0	0	0	0 1 7	15
1	0	0	0	0	1	0	1	0 2 0	16
1	0	0	0	1	0	1	0	0 2 1	17
1	0	0	1	1	0	0	1	0 2 2	18
1	0	1	0	1	0	1	0	0 2 3	19
1	1	0	0	0	0	0	0	0 2 4	20
1	1	0	1	1	0	0	0	0 2 5	21
0	0	0	0	0	0	0	0	0 2 6	22
0	0	0	0	0	0	0	0	0 2 7	23
0	0	1	0	0	1	1	0	0 3 0	24
0	1	0	0	0	0	0	0	0 3 1	25
0	1	0	1	0	0	1	0	0 3 2	26
0	1	1	0	0	1	0	0	0 3 3	27
0	1	1	1	0	1	0	0	0 3 4	28
0	1	1	1	1	0	1	0	0 3 5	29
0	1	1	1	1	1	1	1	0 3 6	30
0	1	1	1	1	1	1	1	0 3 7	31

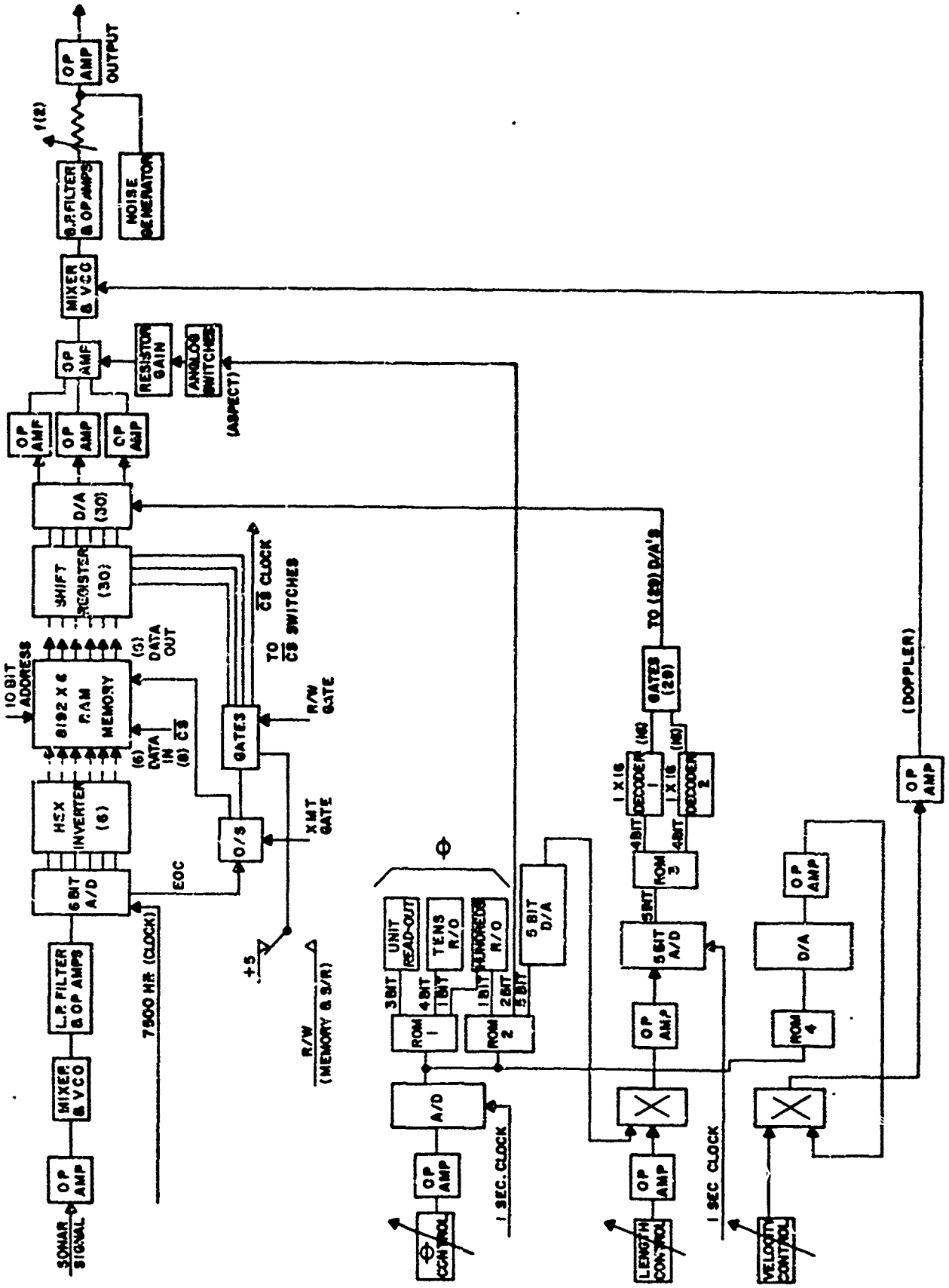


FIGURE 1. SYSTEM BLOCK DIAGRAM

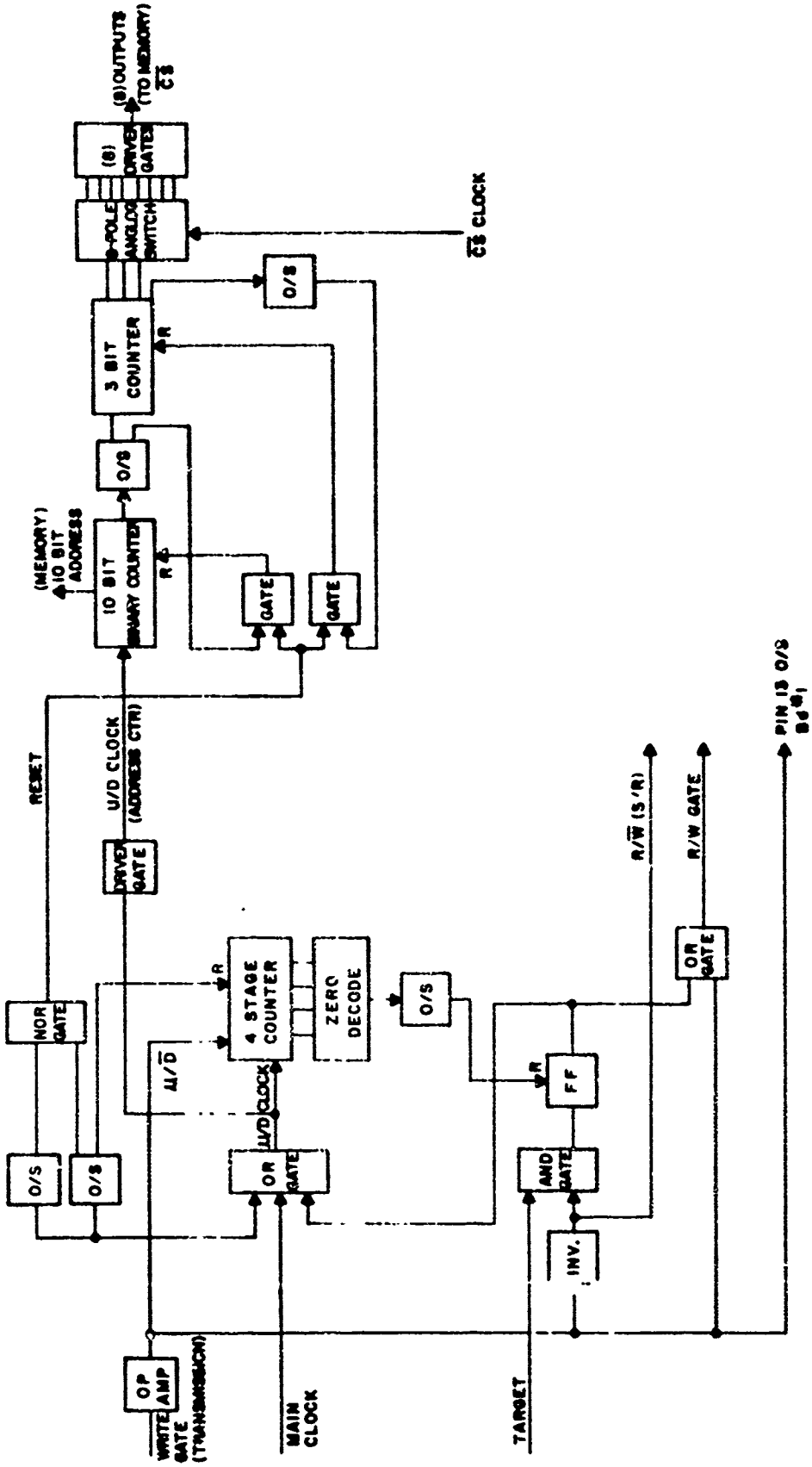


FIGURE 2 TIMING CONTROL BLOCK DIAGRAM

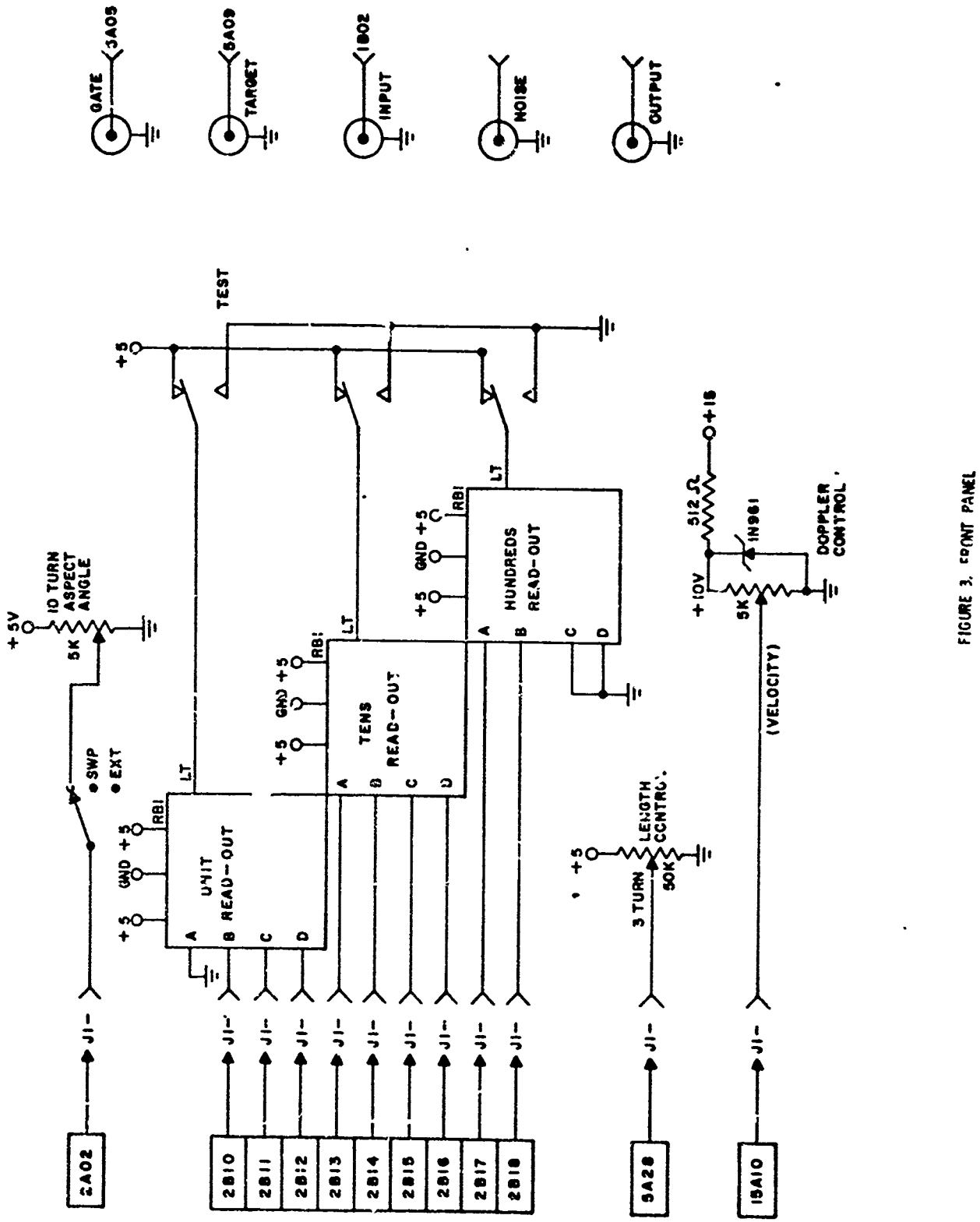


FIGURE 3. FRONT PANEL

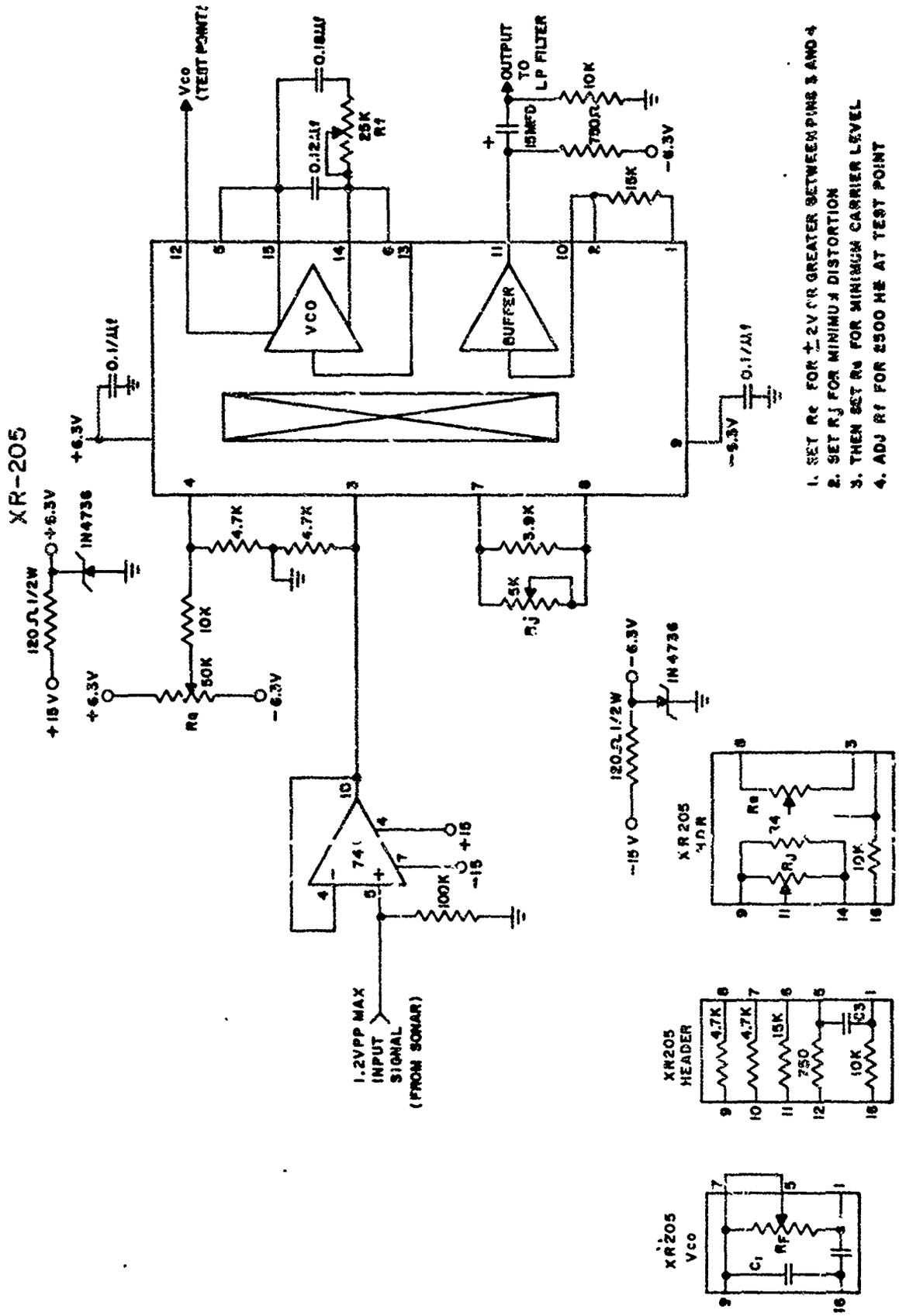


FIGURE 4. INPUT MIXER/OSCILLATOR

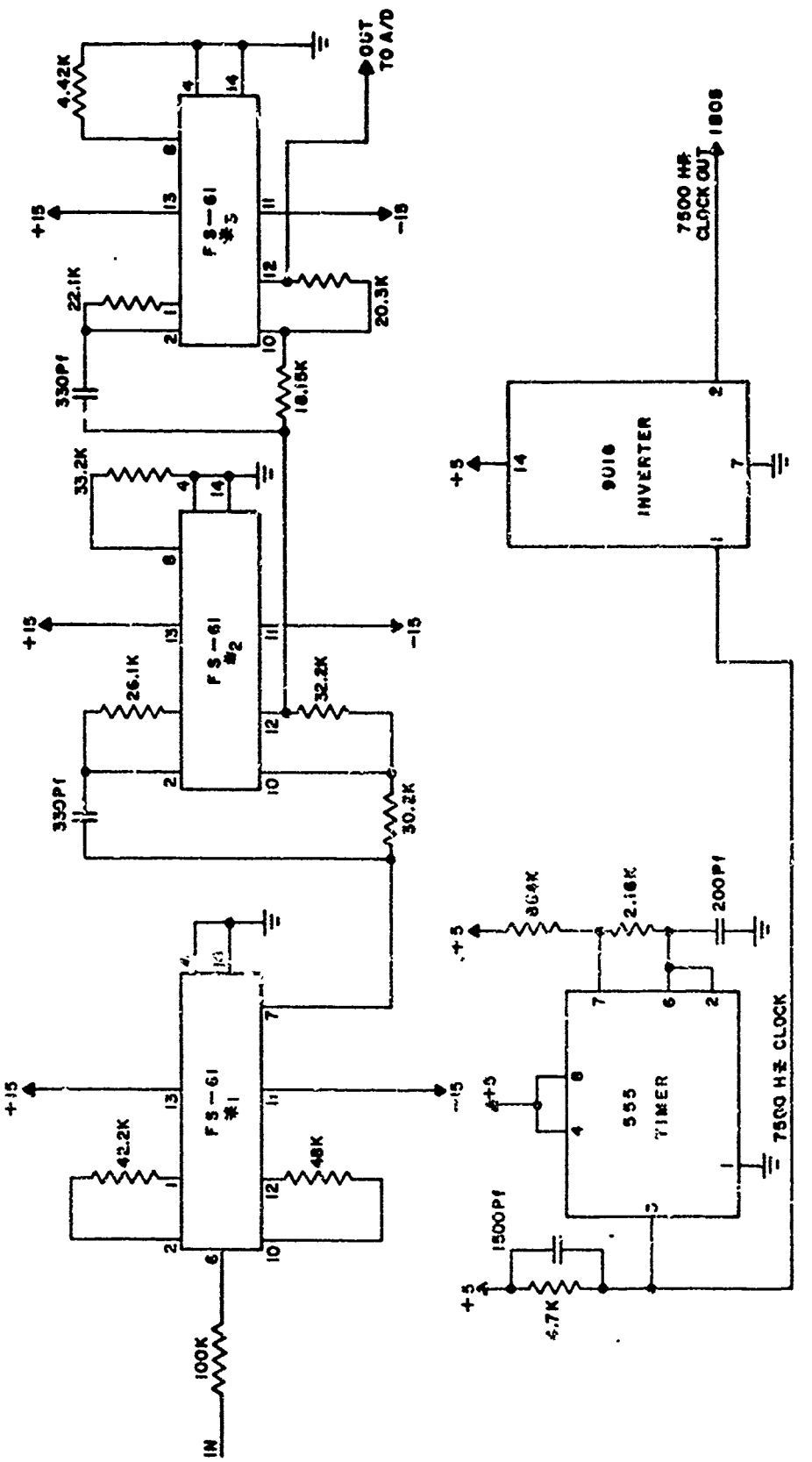


FIGURE 5. LO 'SS FILTER AND CLOCK

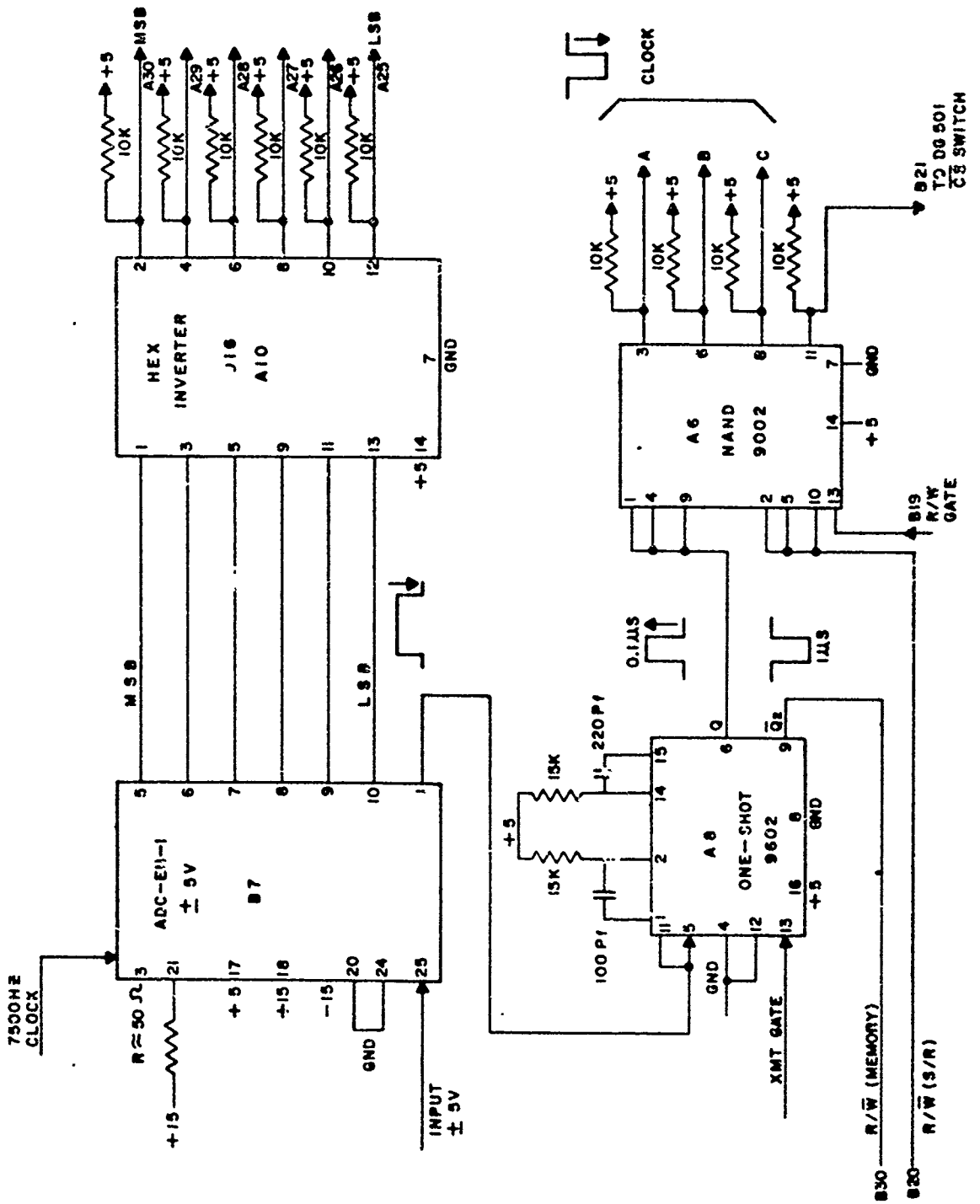


FIGURE 6. INPUT DIGITIZING CIRCUIT

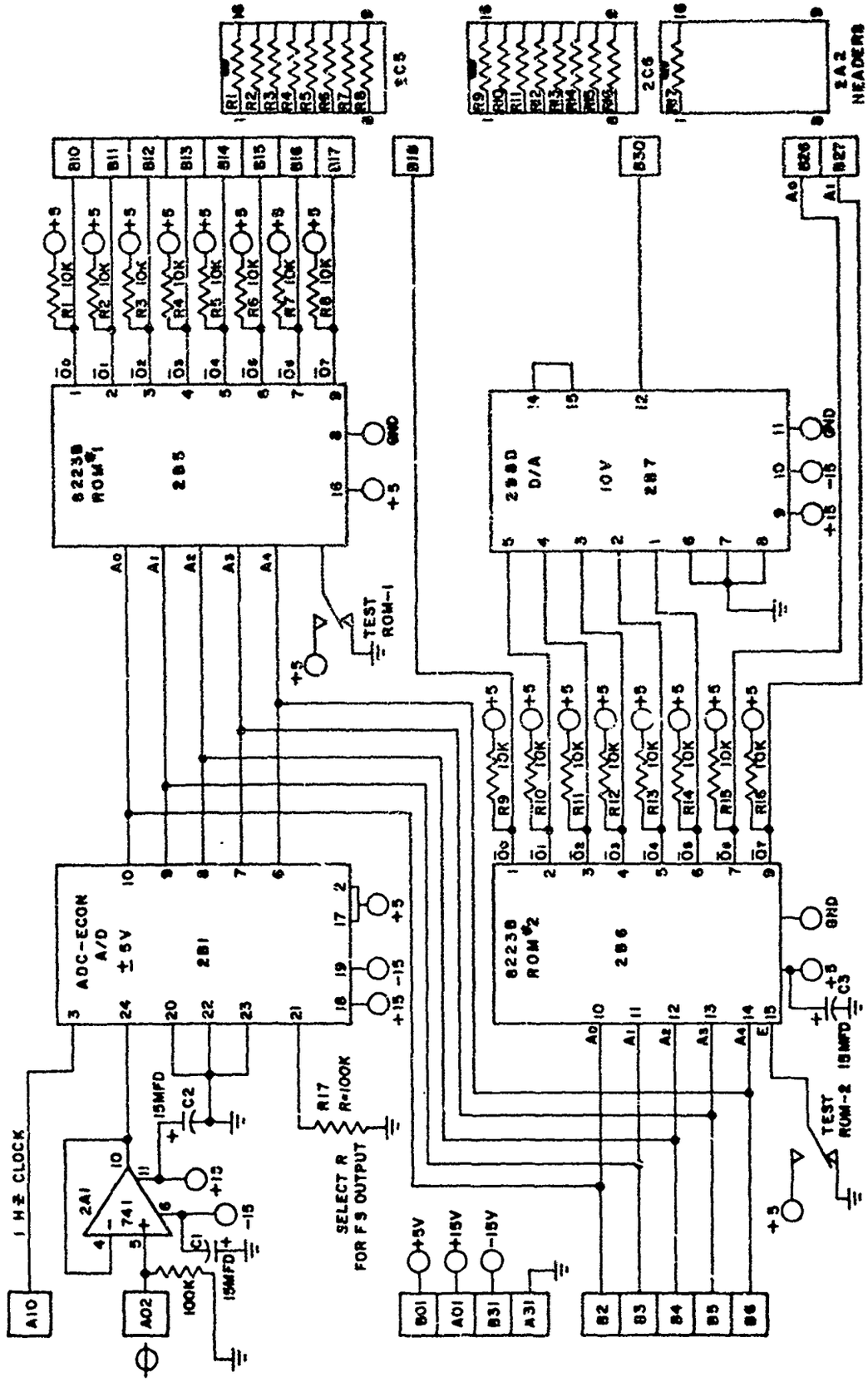


FIGURE 7. ASP. ANGLE CIRCUIT

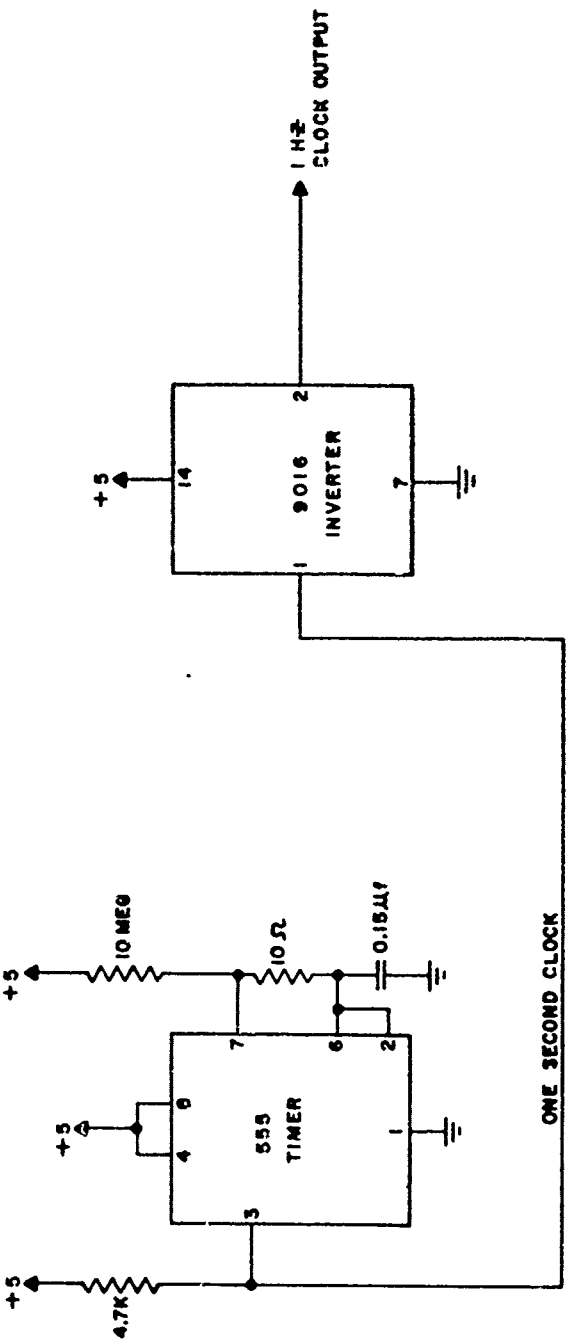


FIGURE 8. ONE-SECOND CLOCK

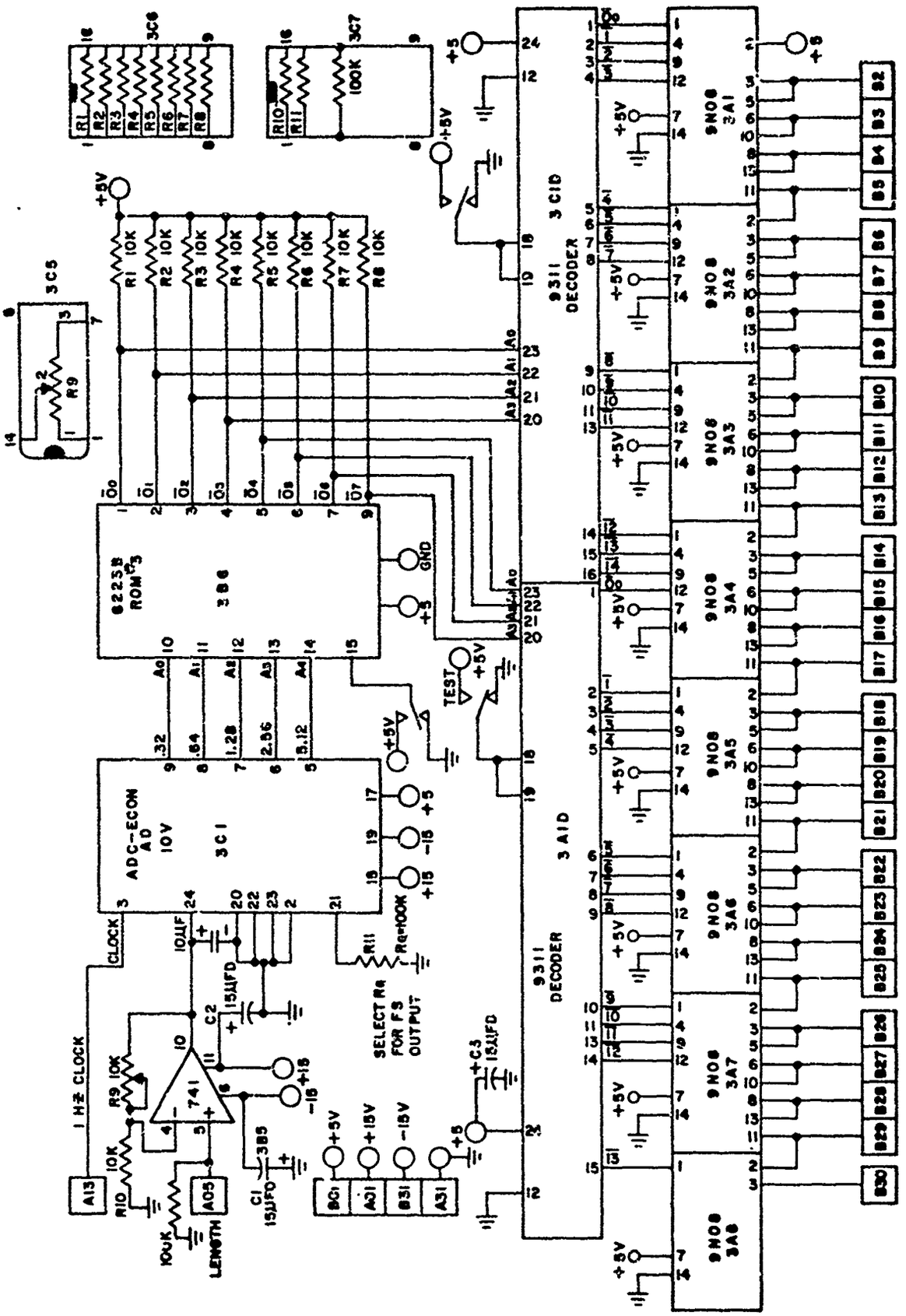


FIGURE COS Φ CONTROL

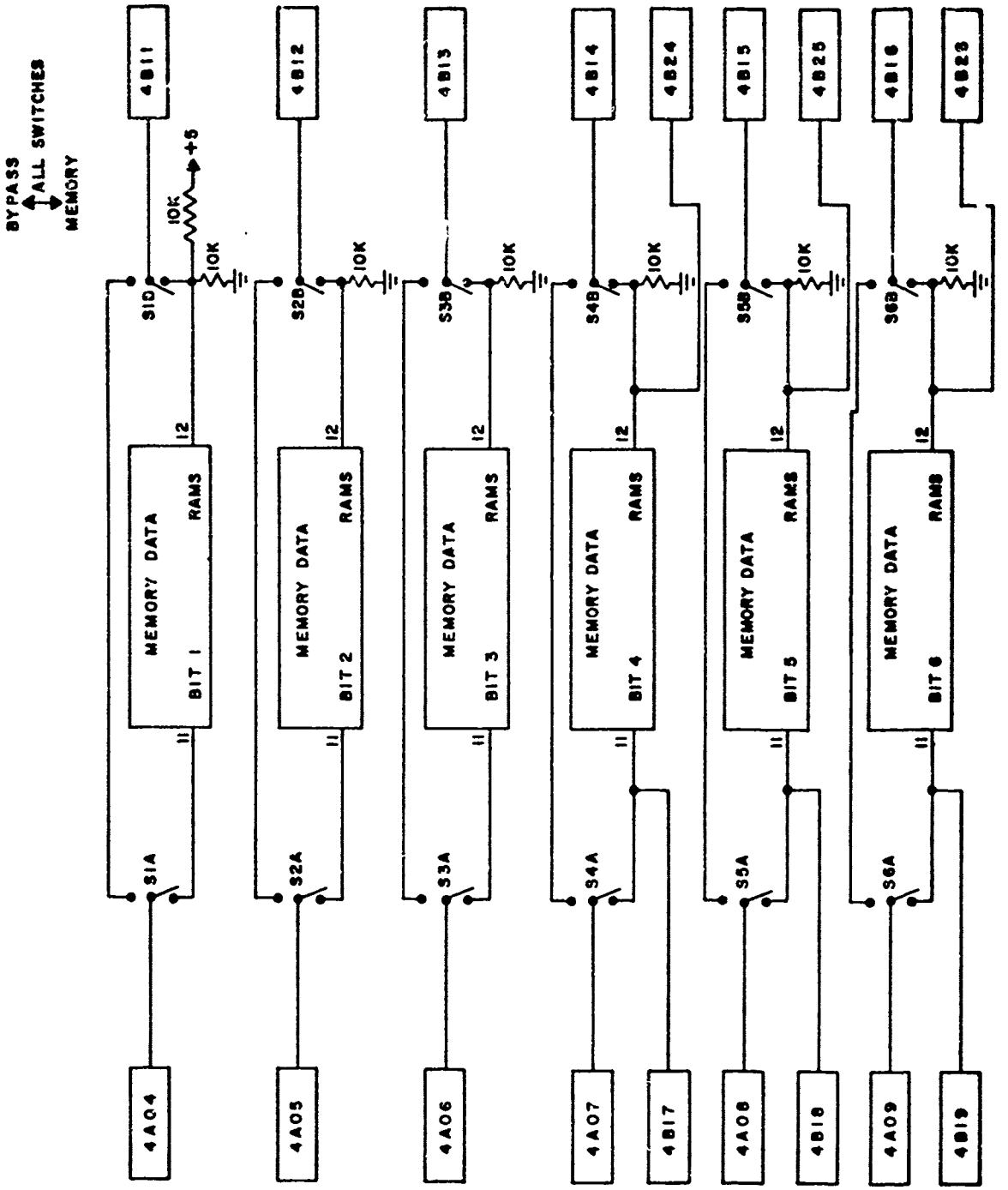


FIGURE 10. MEMORY BY-PASS DIAGRAM

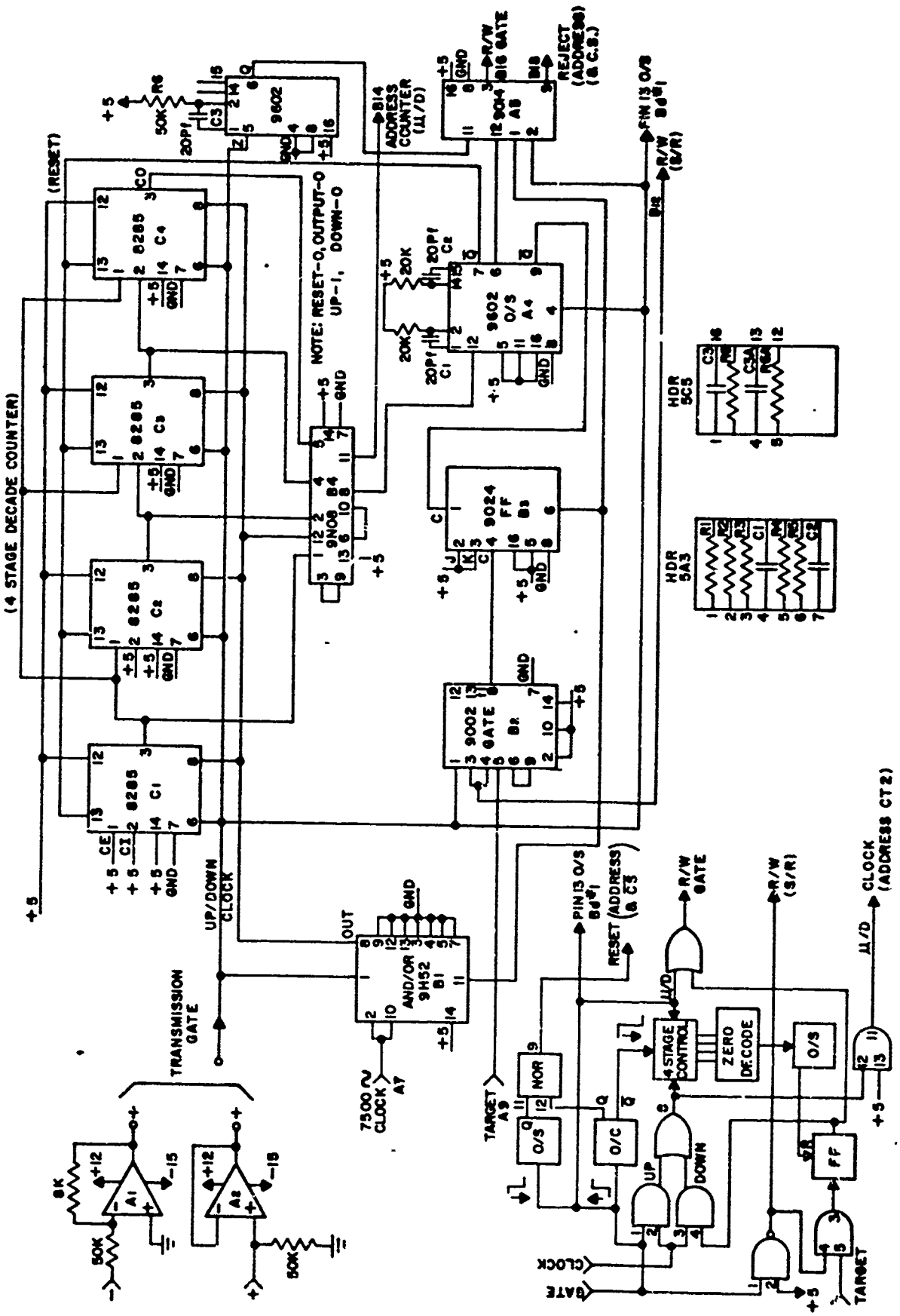


FIGURE 11. TIMING CONTROL

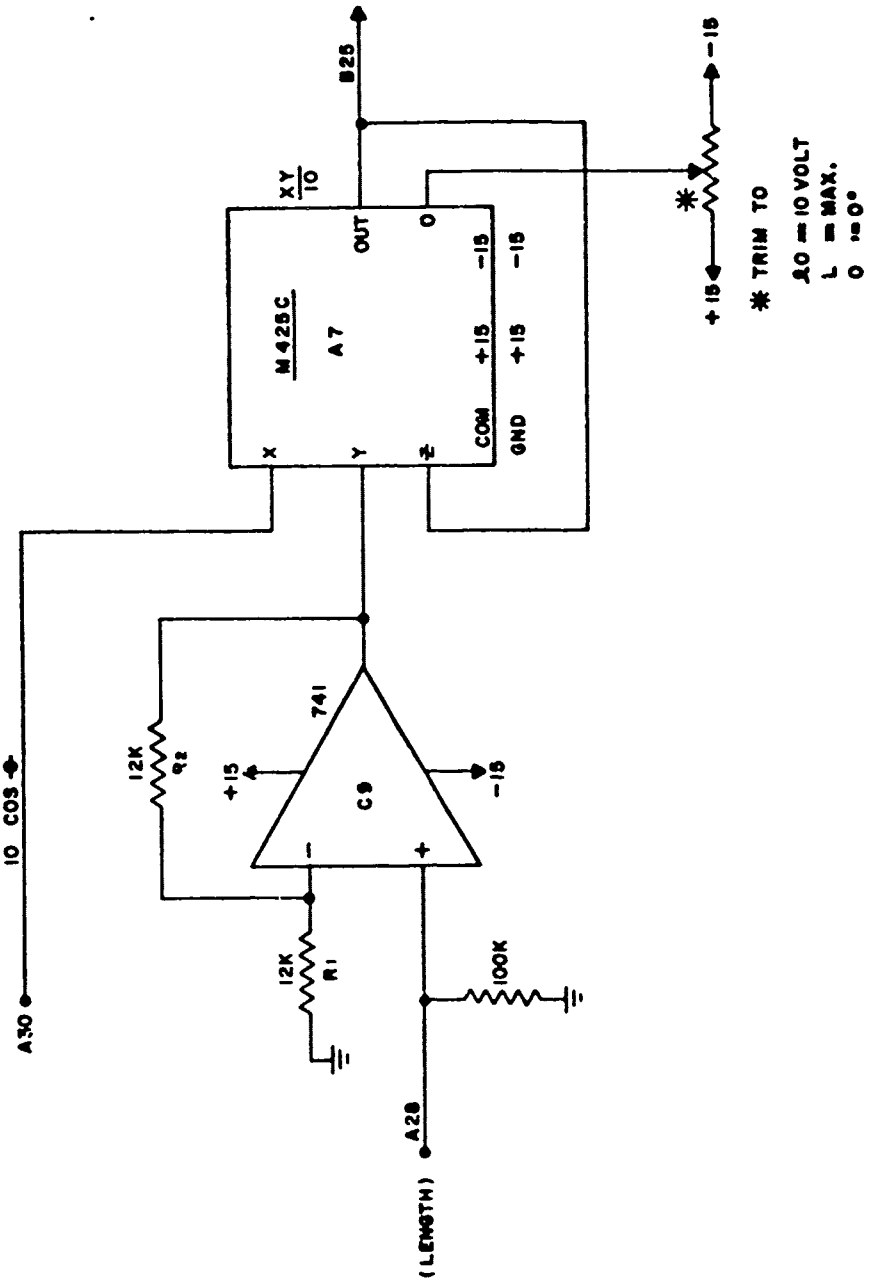


FIGURE 12. LCOS ◆ MULTIPLIER

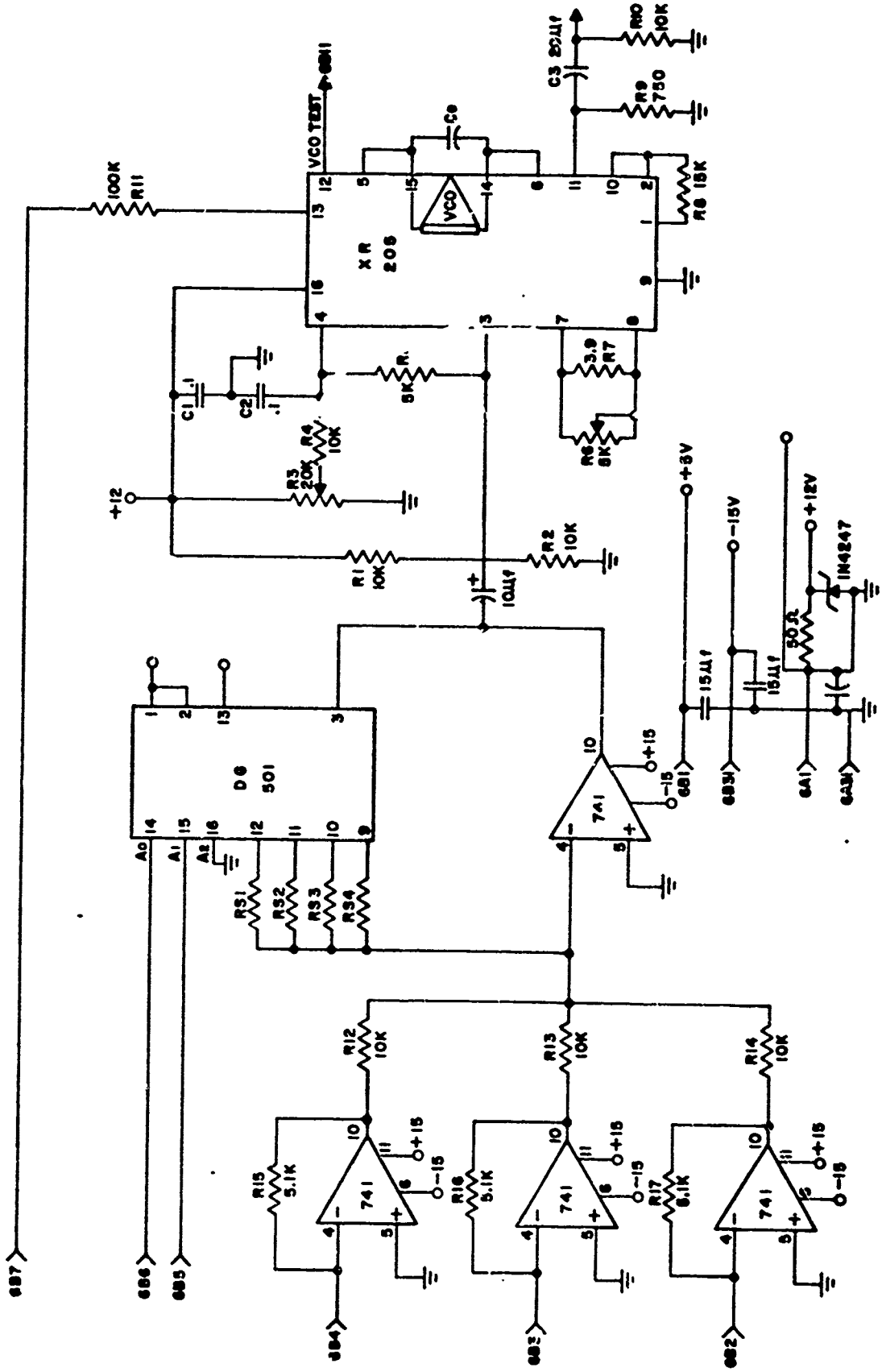


FIGURE 13. OUTPUT CIRCUITRY

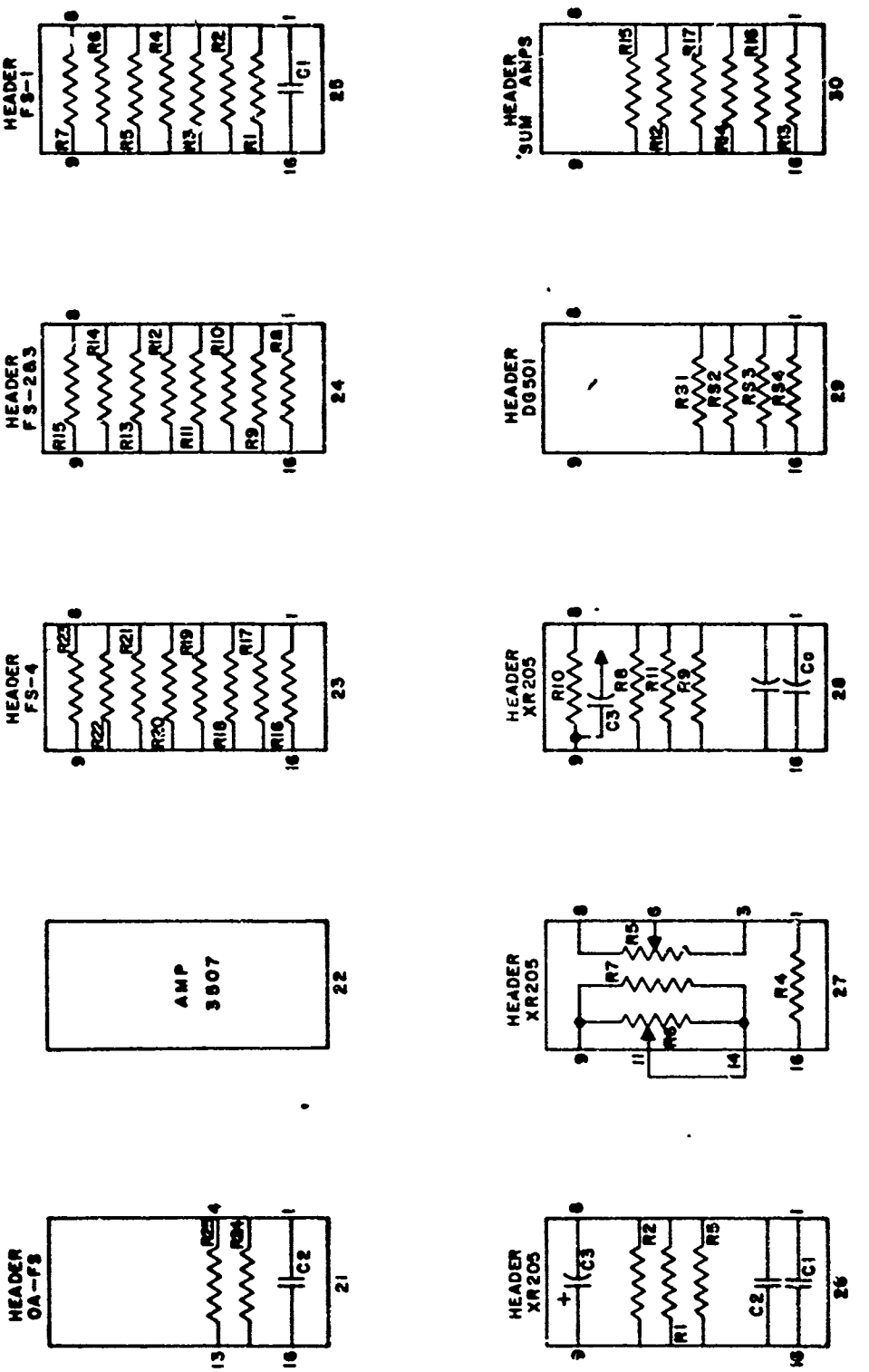


FIGURE 14. HEADERS/CARD 6

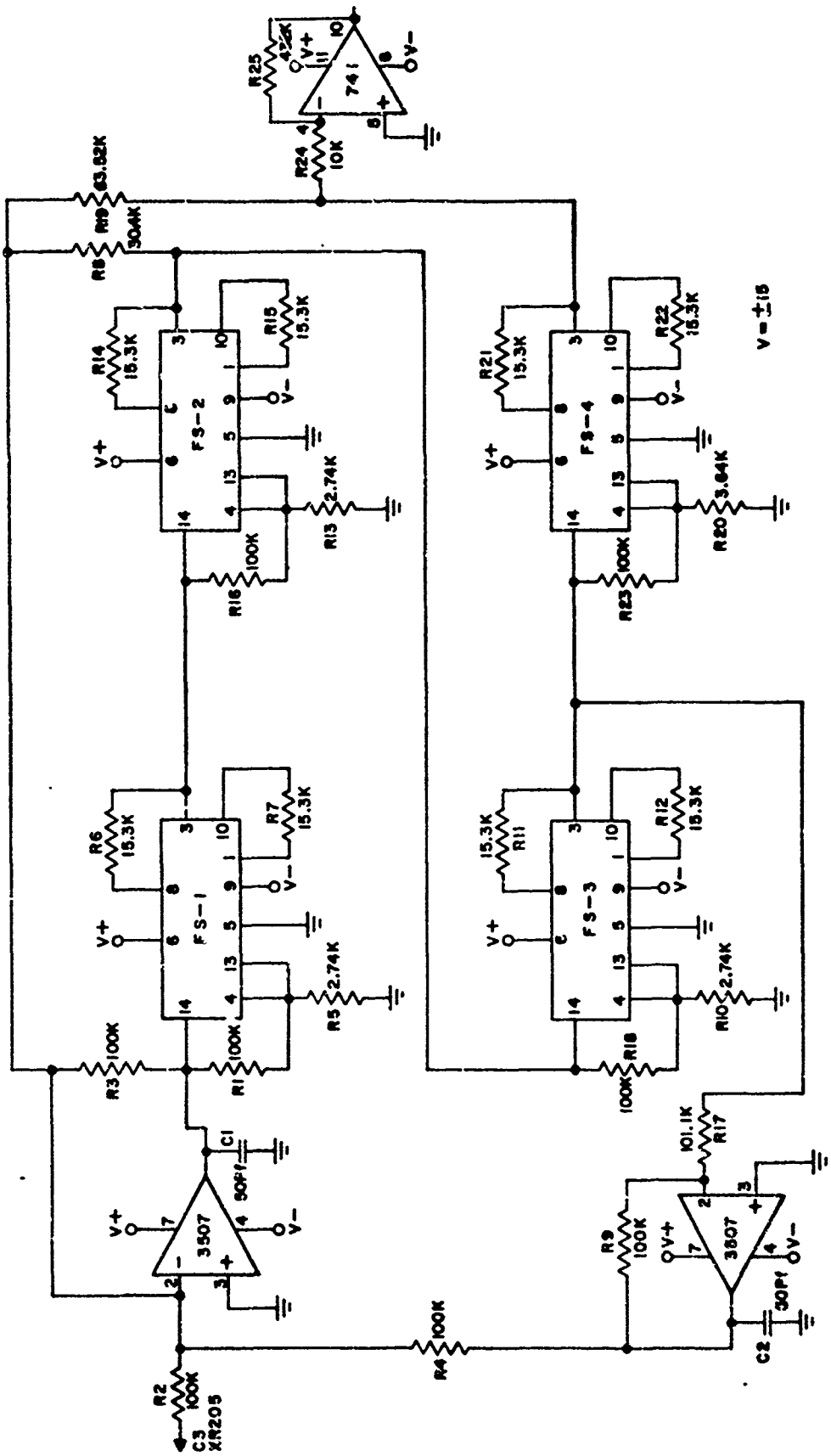
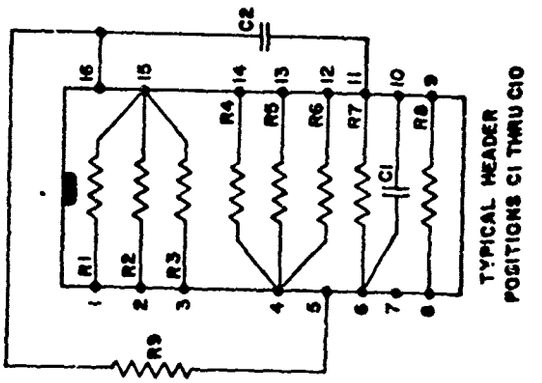


FIGURE 15. BAND-PASS FILTER



TO CONTINUATION OF SHIFT REGISTER CIRCUIT
(TO *3 SECTION)

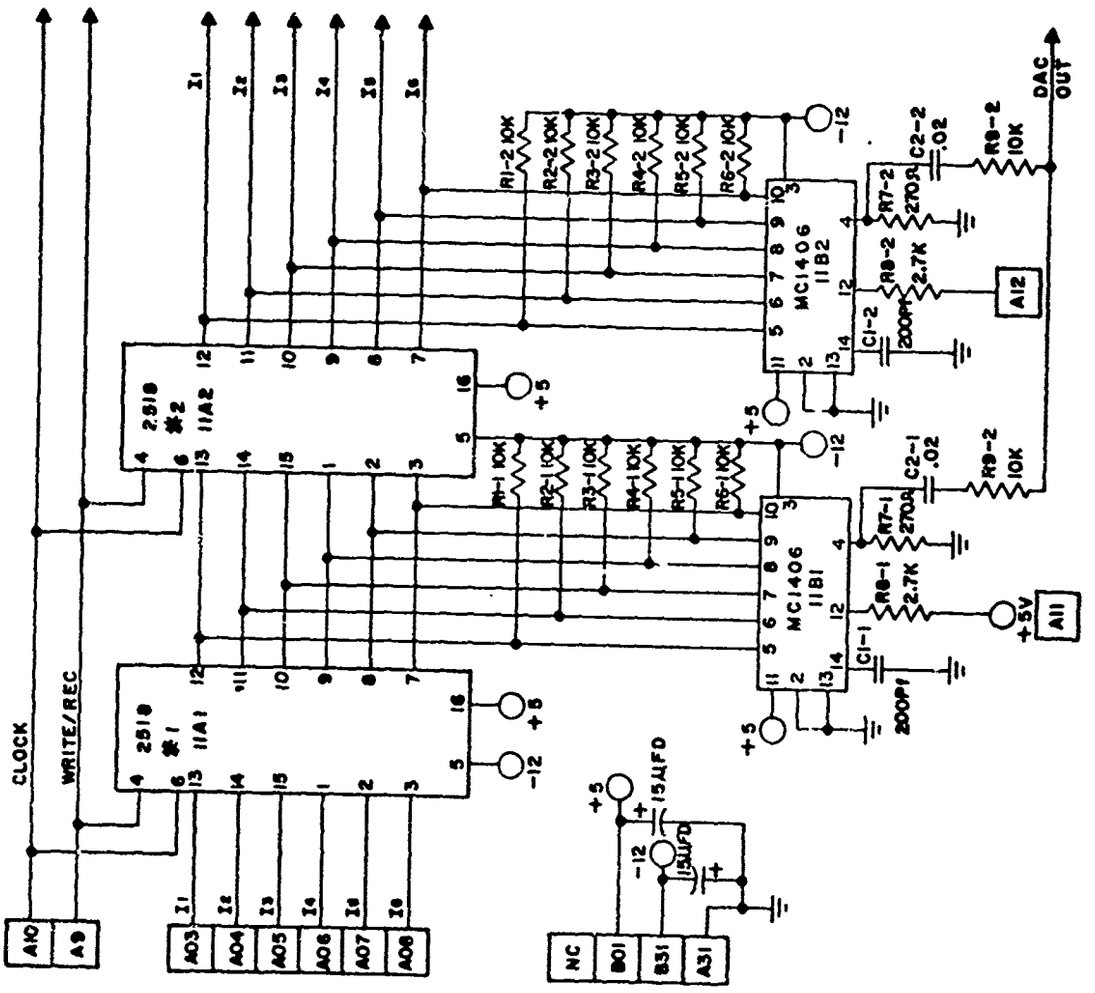


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13

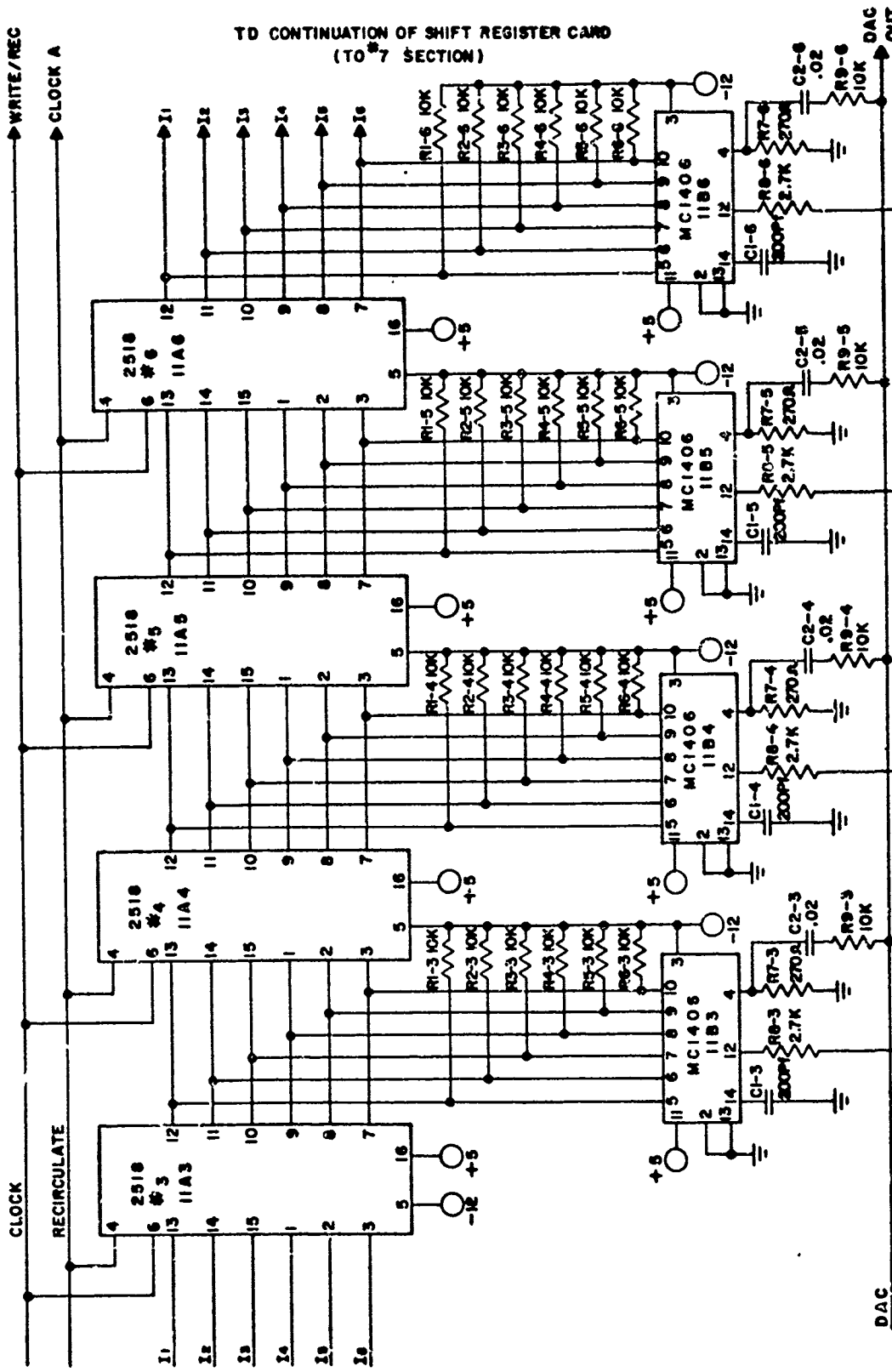


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13

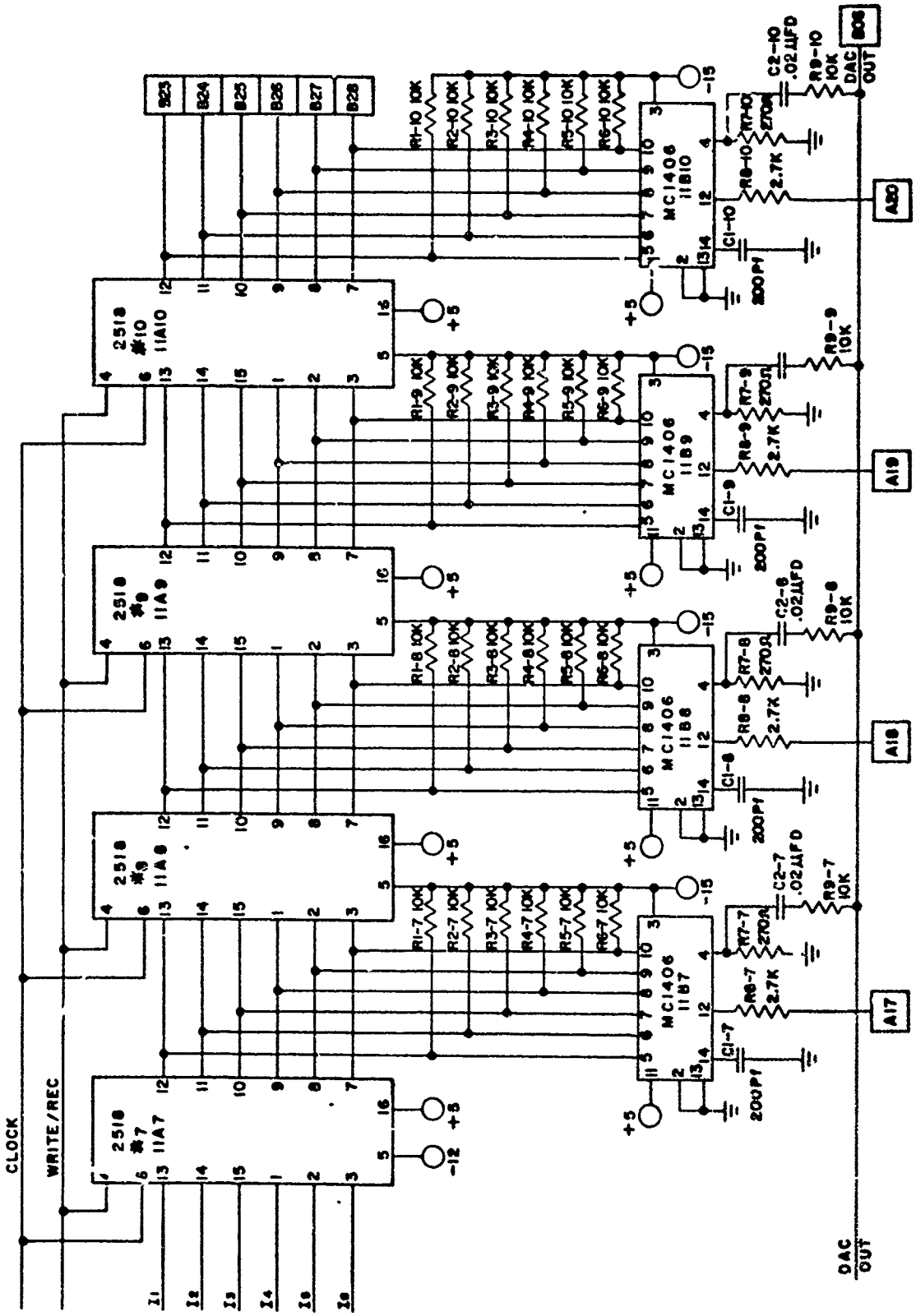
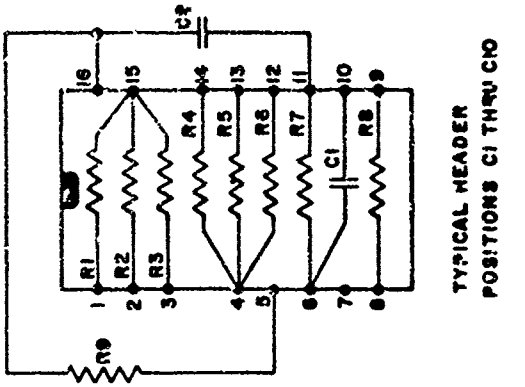


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13



TO CONTINUATION OF SHIFT REGISTER CIRCUIT (TO SHEET 3 SECTION)

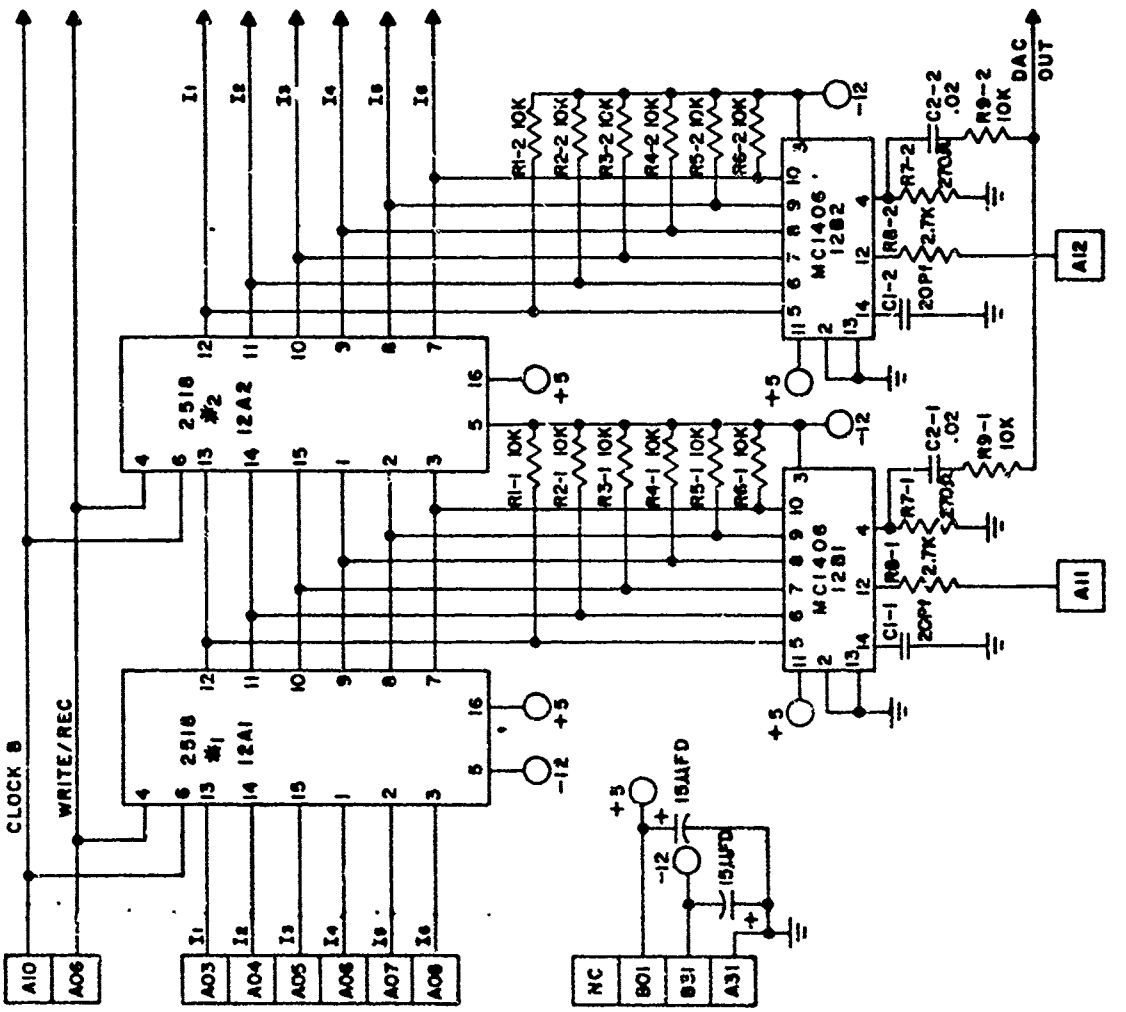


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13

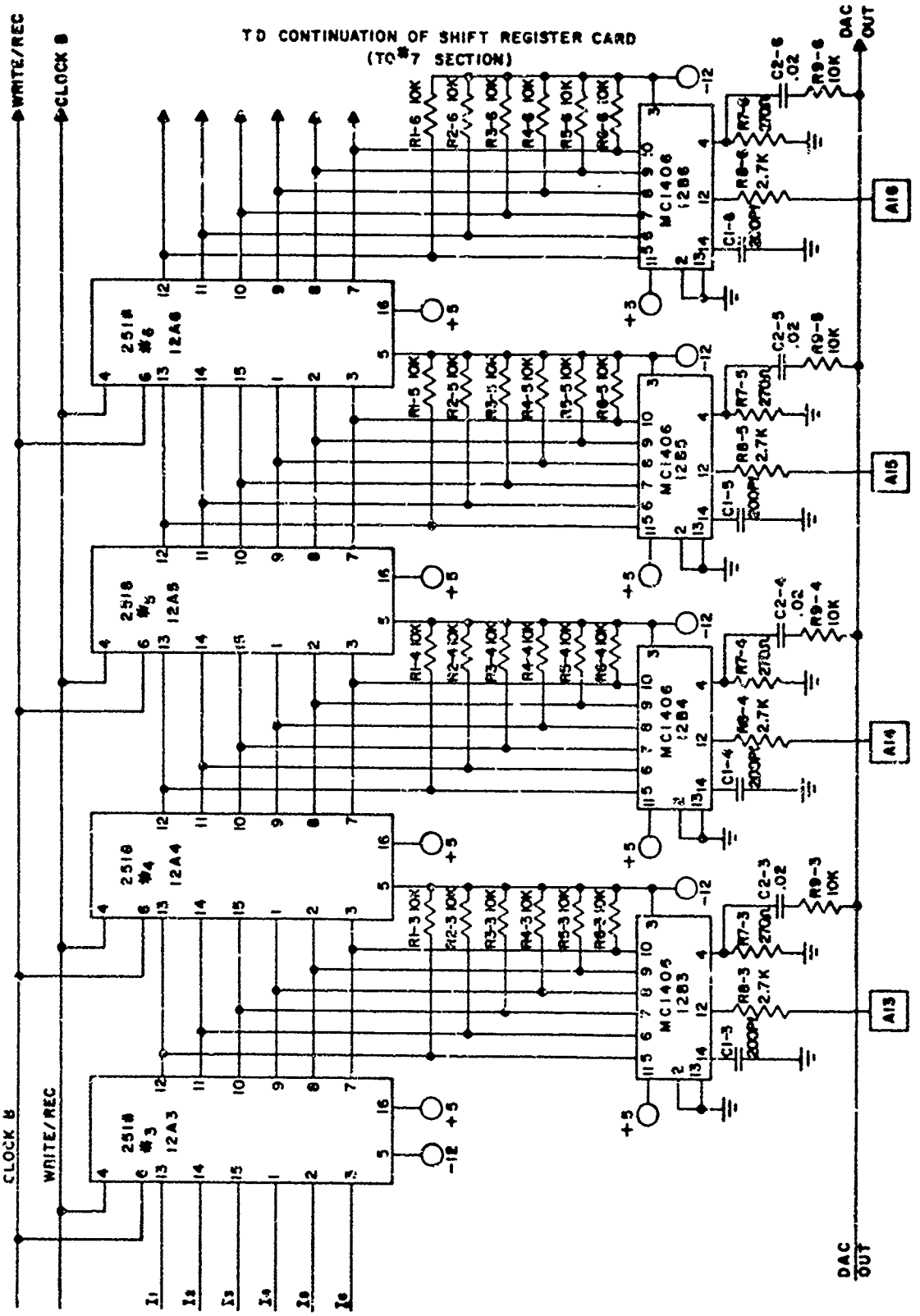


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13

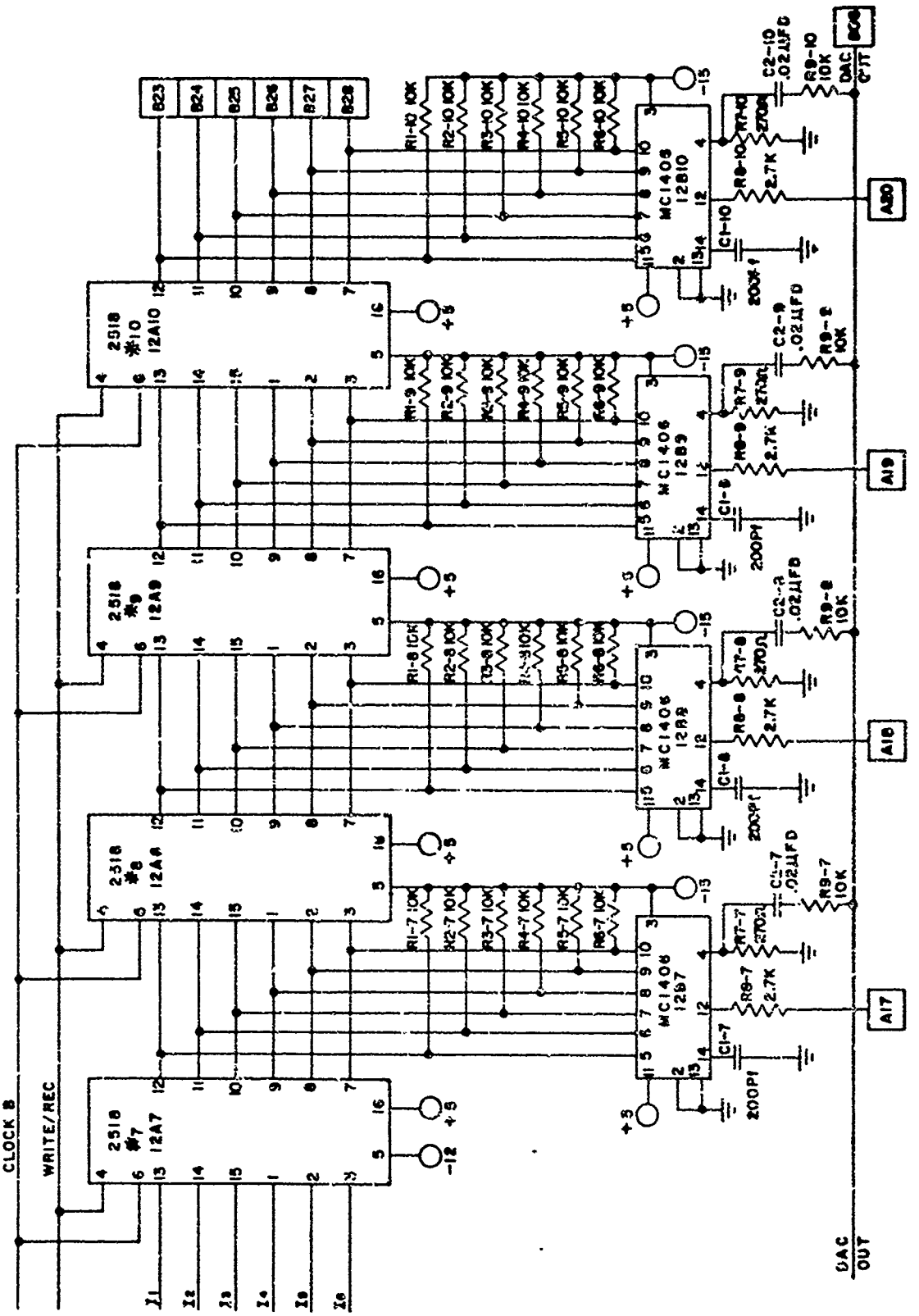


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13

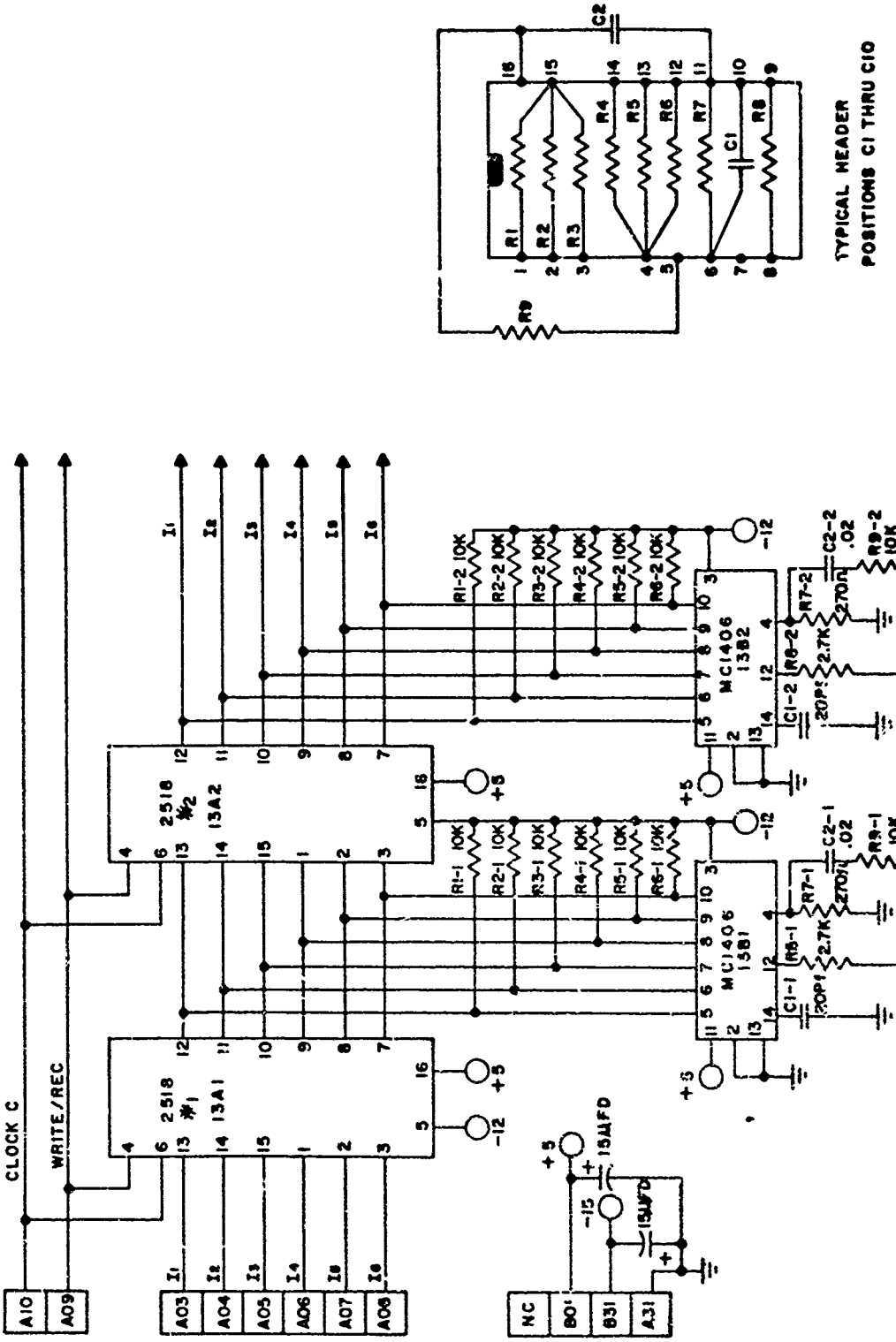


FIGURE 13. SHIFT REGISTERS-CARDS 11, 12, 13

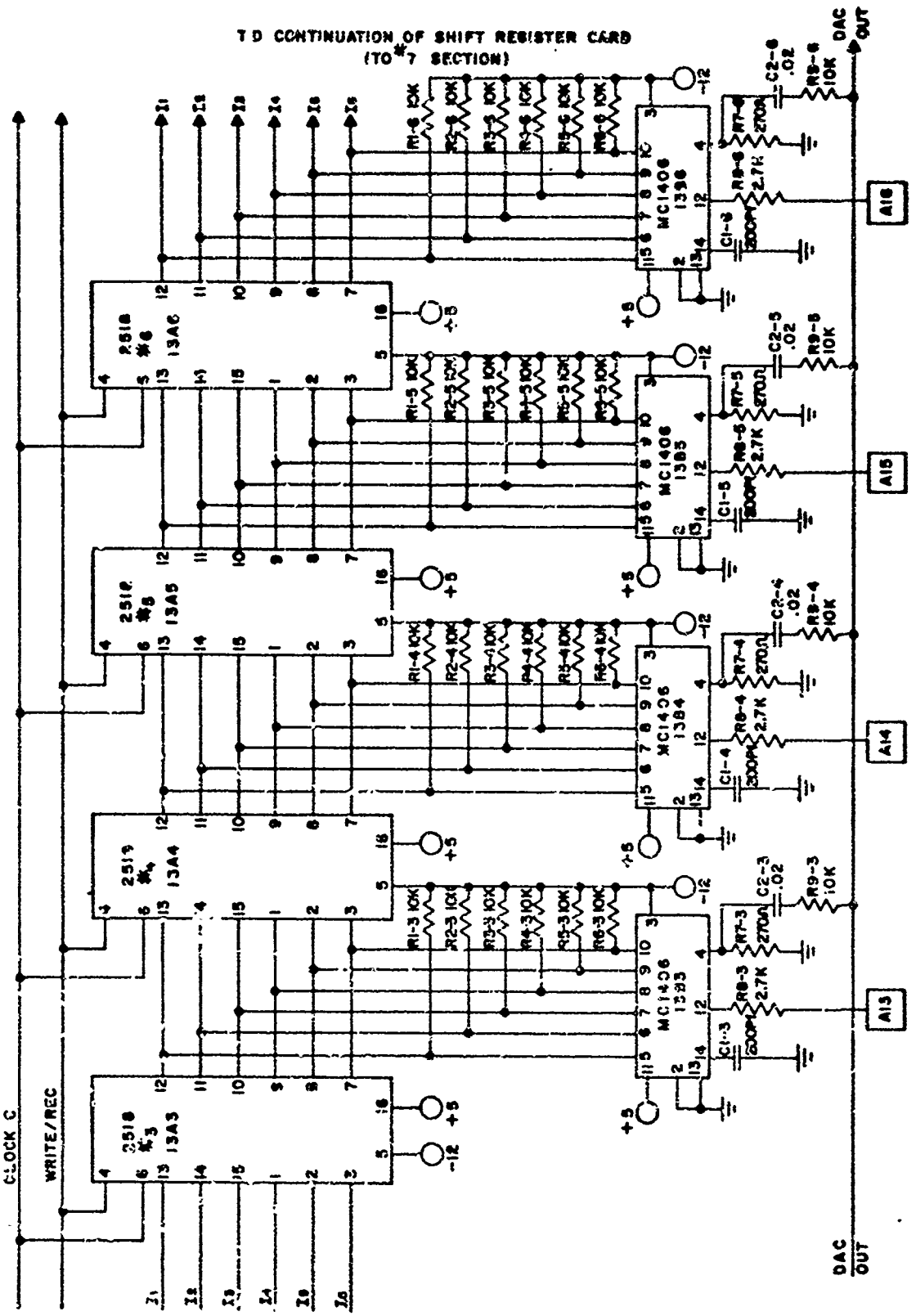


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13

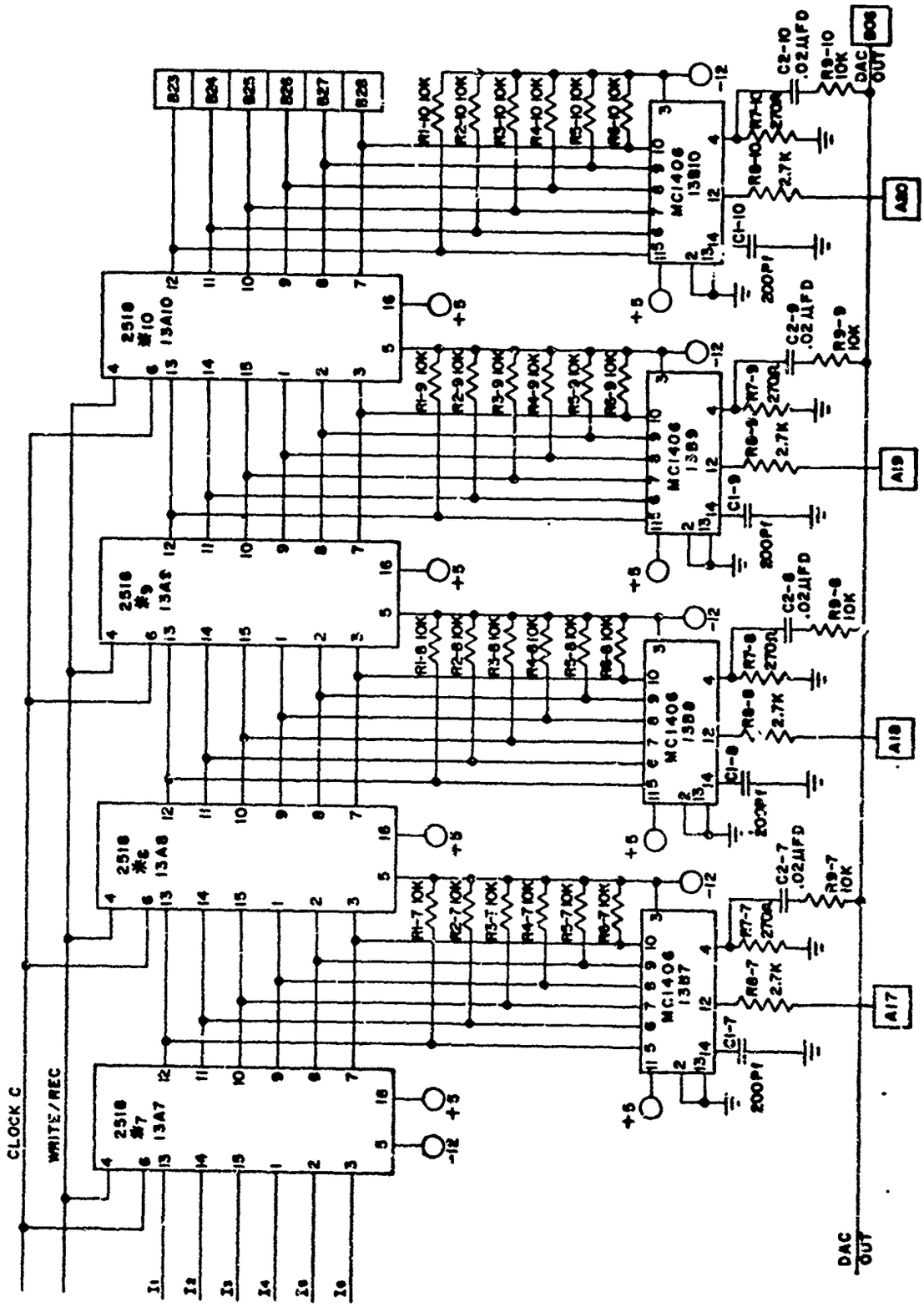


FIGURE 16. SHIFT REGISTERS-CARDS 11, 12, 13

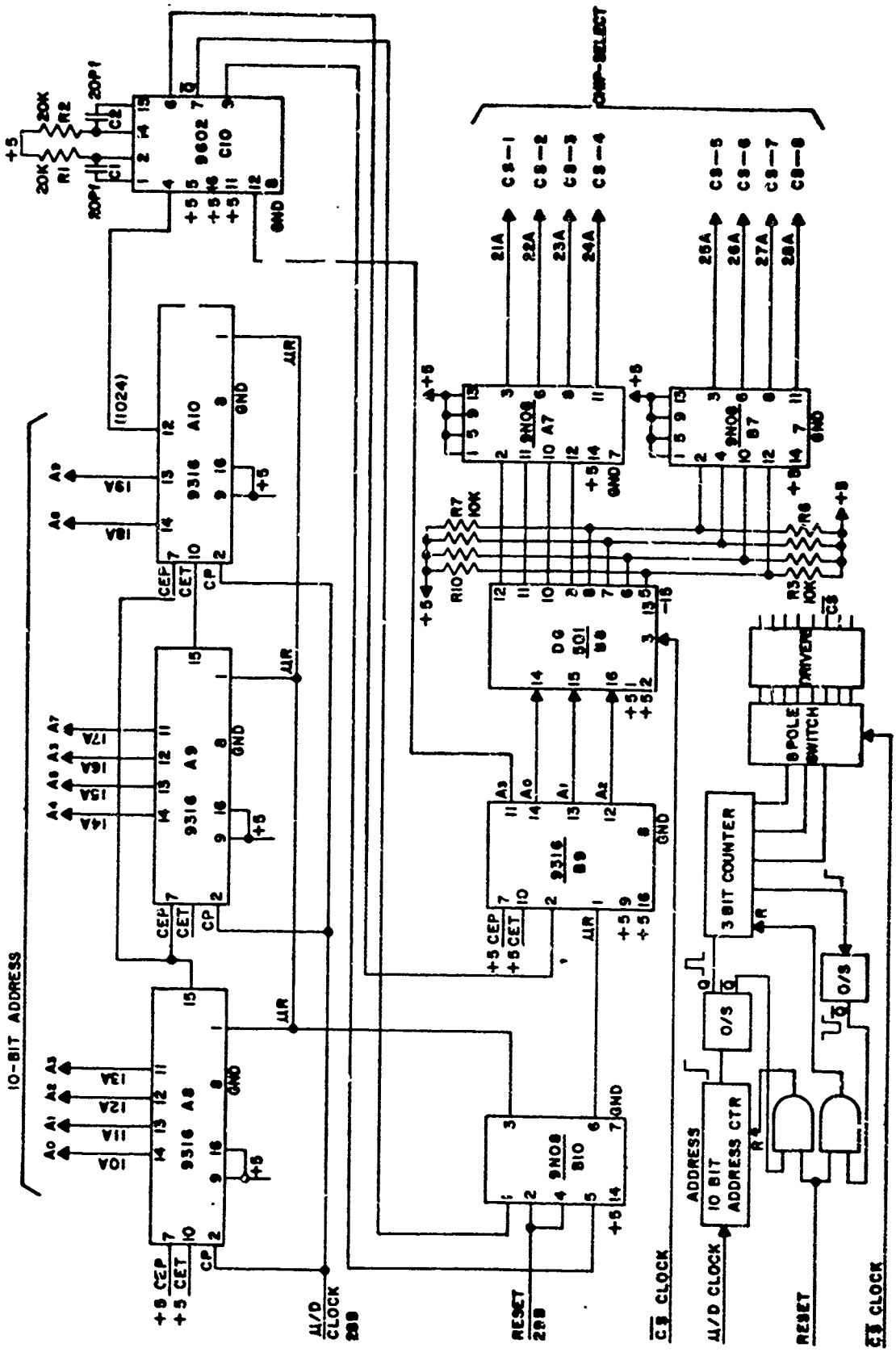


FIGURE 17. RAM ADDRESS

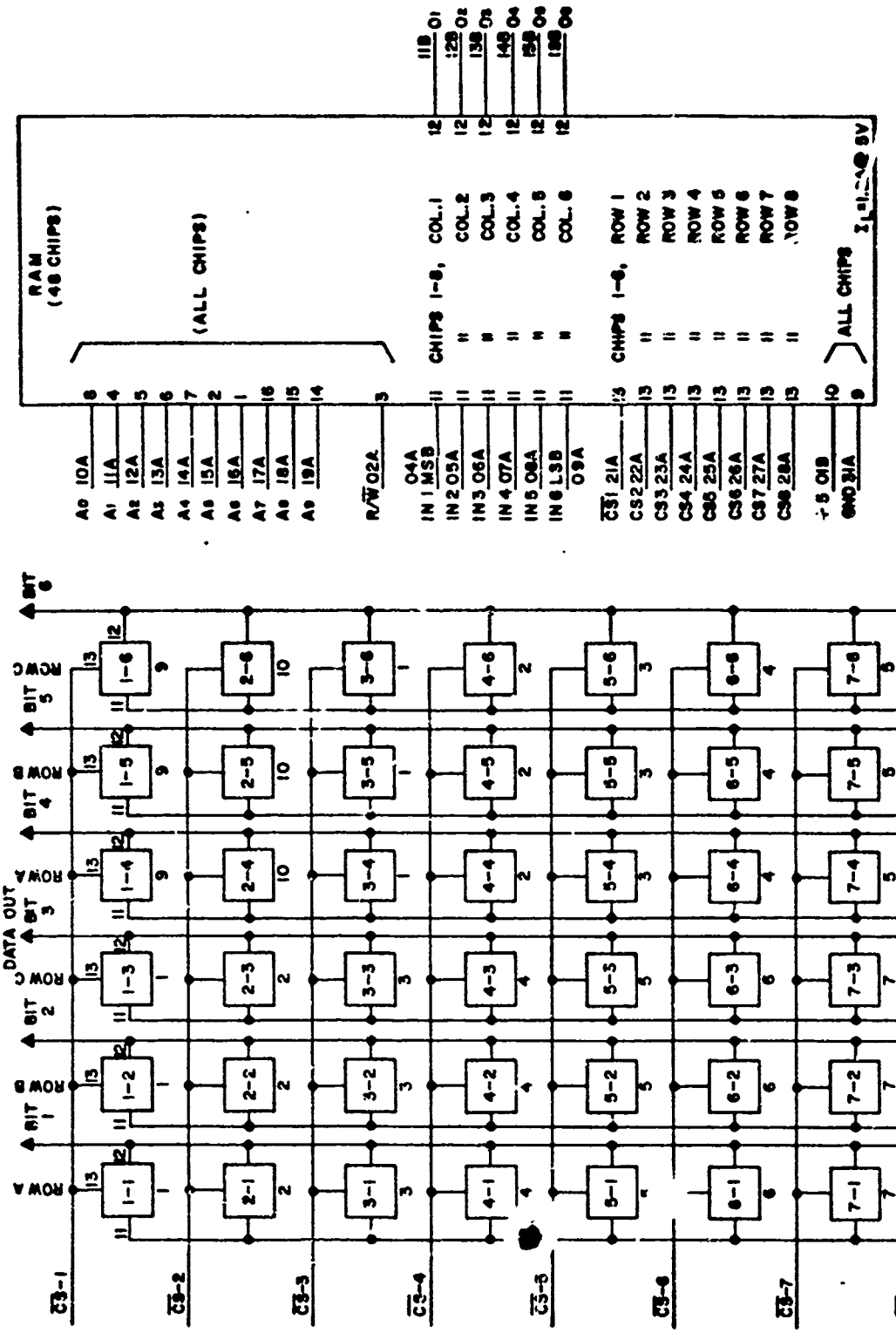


FIGURE 18. 8192 X 6 MEMORY

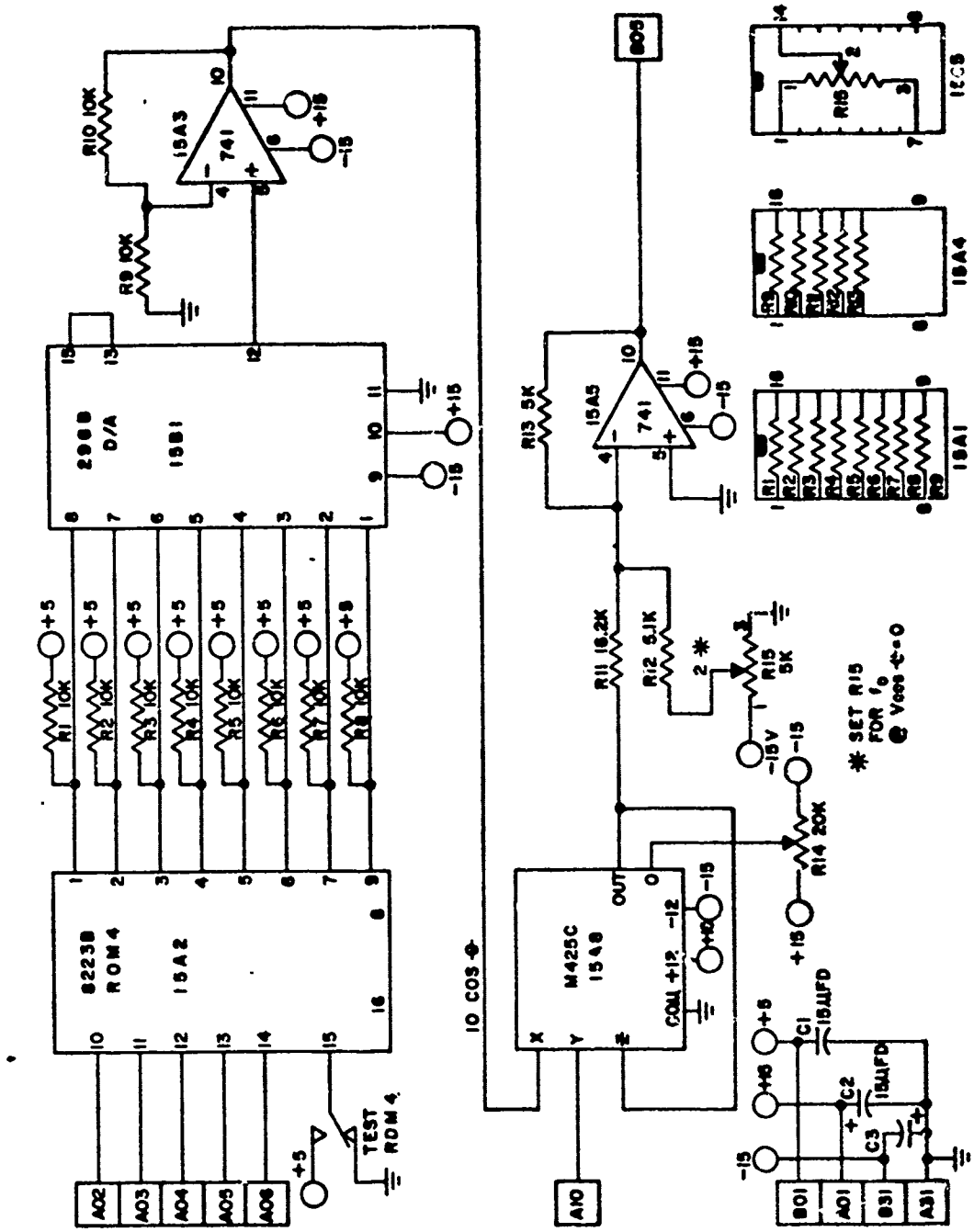


FIGURE 19. DOPPLER CONTROL

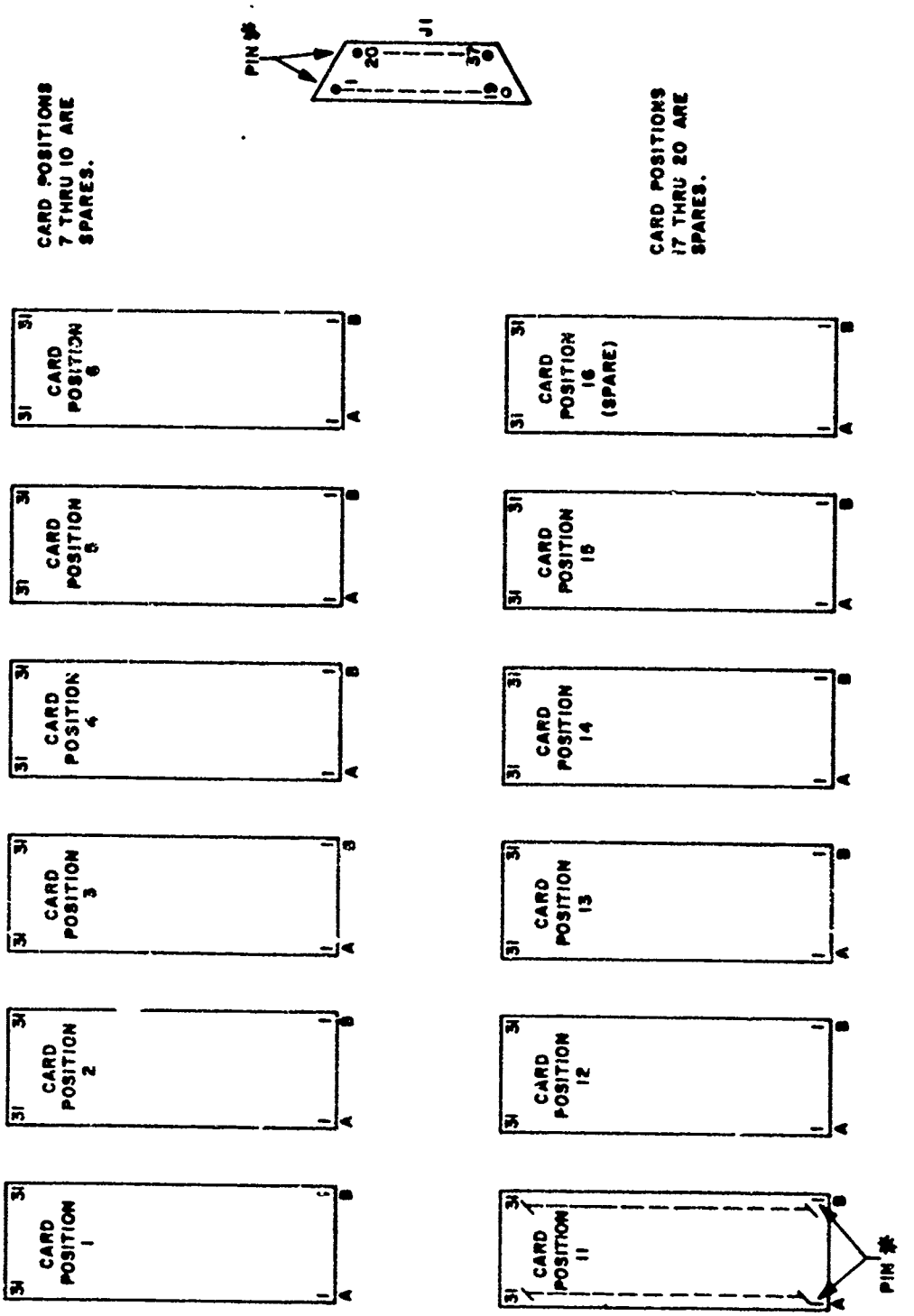


FIGURE 20. CARD POSITIONS

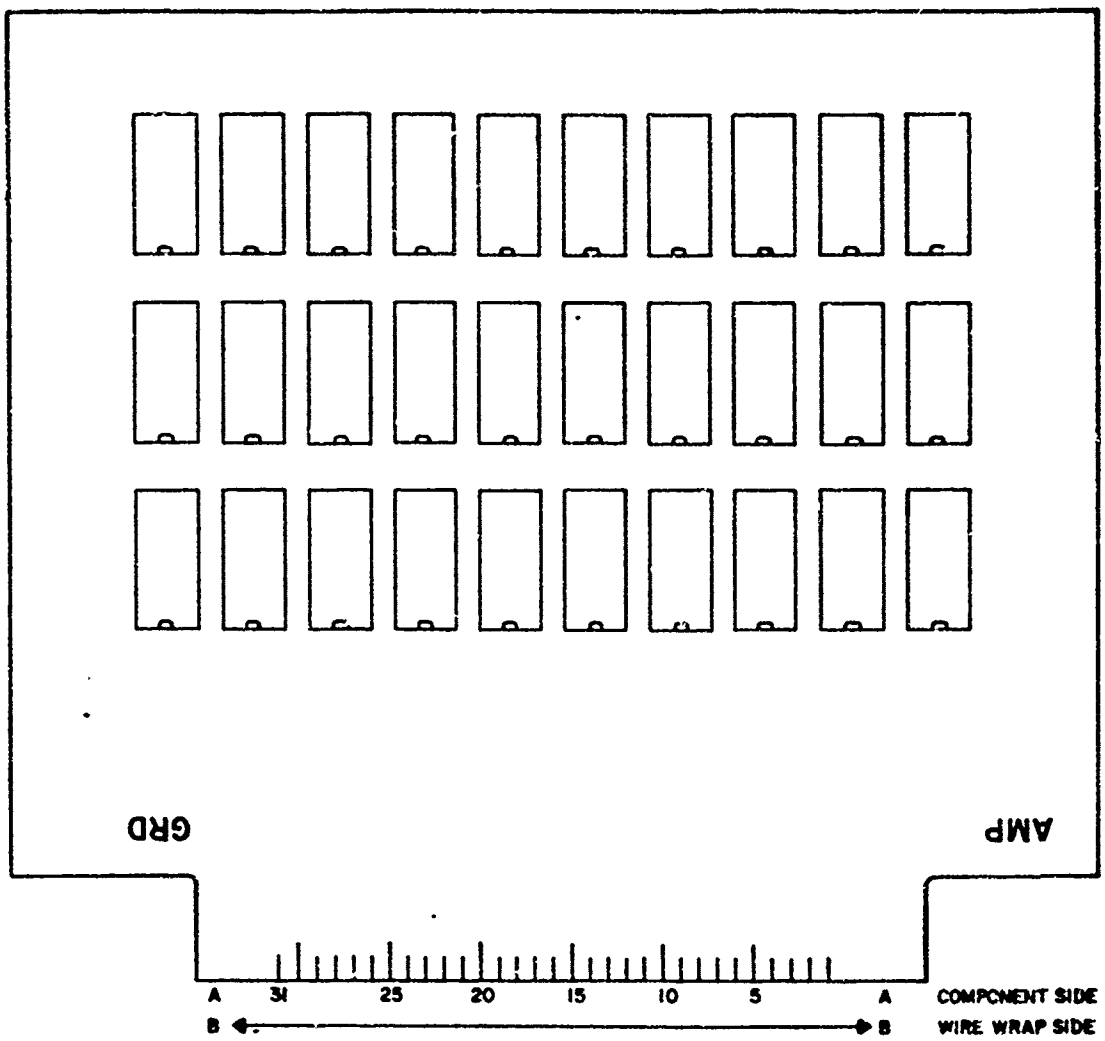


FIGURE 2' SAMPLE CARD LAYOUT

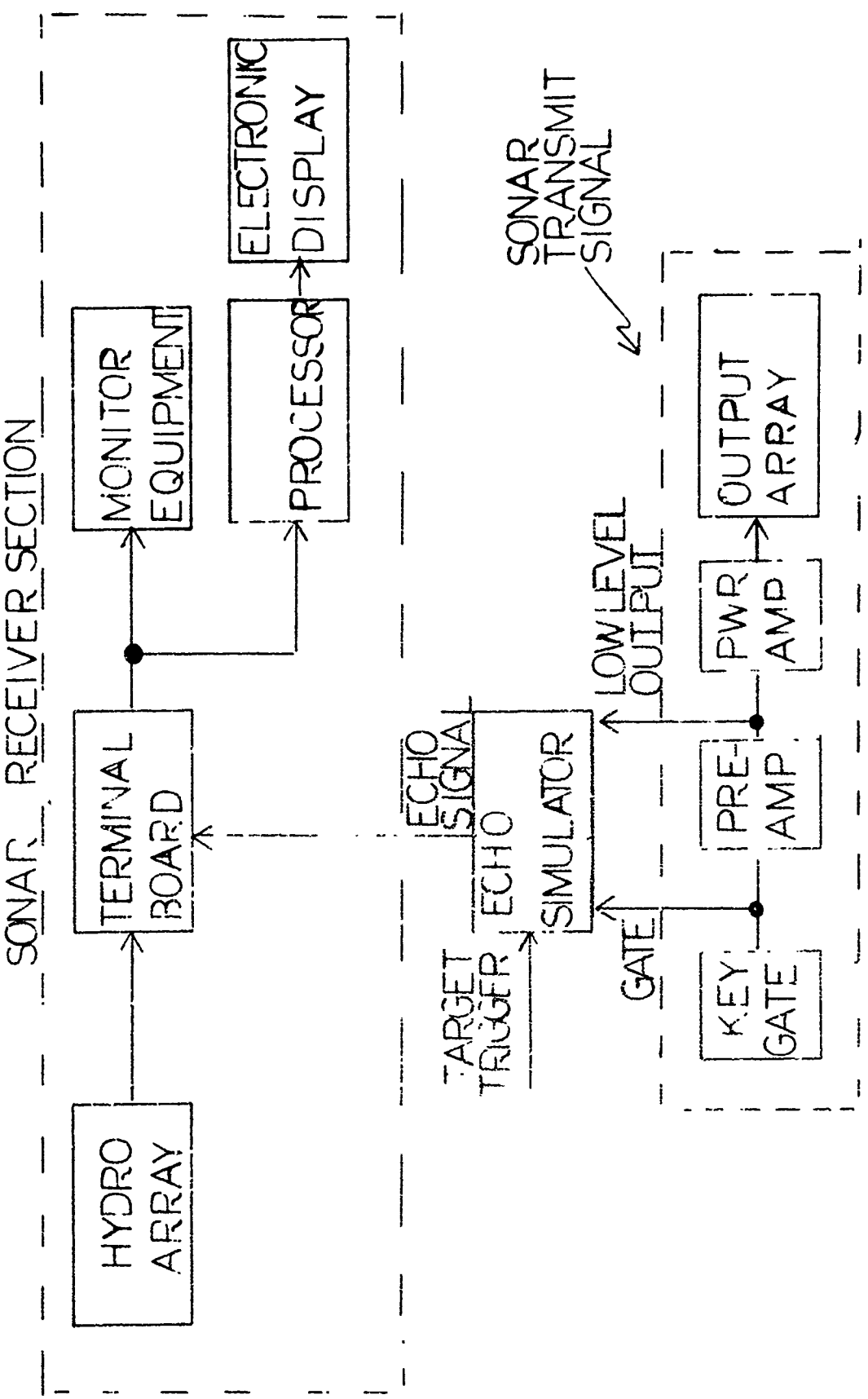


FIGURE 22. INPUT/OUTPUT BLOCK DIAGRAM

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